

### CPU:

INTEL - Haswell LGA1150

### System Chipset:

INTEL - Lynx Point PCH(H81)

### OnBoard Chipset:

Audio: Realtek ALC662

LAN: Realtek RTL8111G

SIO:NUVOTON 6779D

Flash ROM: 64Mb SPI (PCH)

### Main Memory:

Dual channel DDR-III \* 2  
(1333/1600 MHz ; 1/2/4/8GB)

### Expansion Slots:

PCI Express (X16) Slot \* 1

PCI Express (X1) Slot \* 1

PCI Slot \*2 by ASM1083

Mini-PCIE connector \*1

### PWM:

Controller:VRM 12.5 -NCP81102MNTX 3 Phase  
NCP1587GDR2G for DDR3\_+1.5V (1 Phase)

### Other:

SATA2.0\*2

SATA3.0\*2

USB2.0 Rear\*4

USB2.0 Front\*2

USB3.0 Front\*2

VGA/HDMI/DISPLAY

TPM Header \*1(debug only)

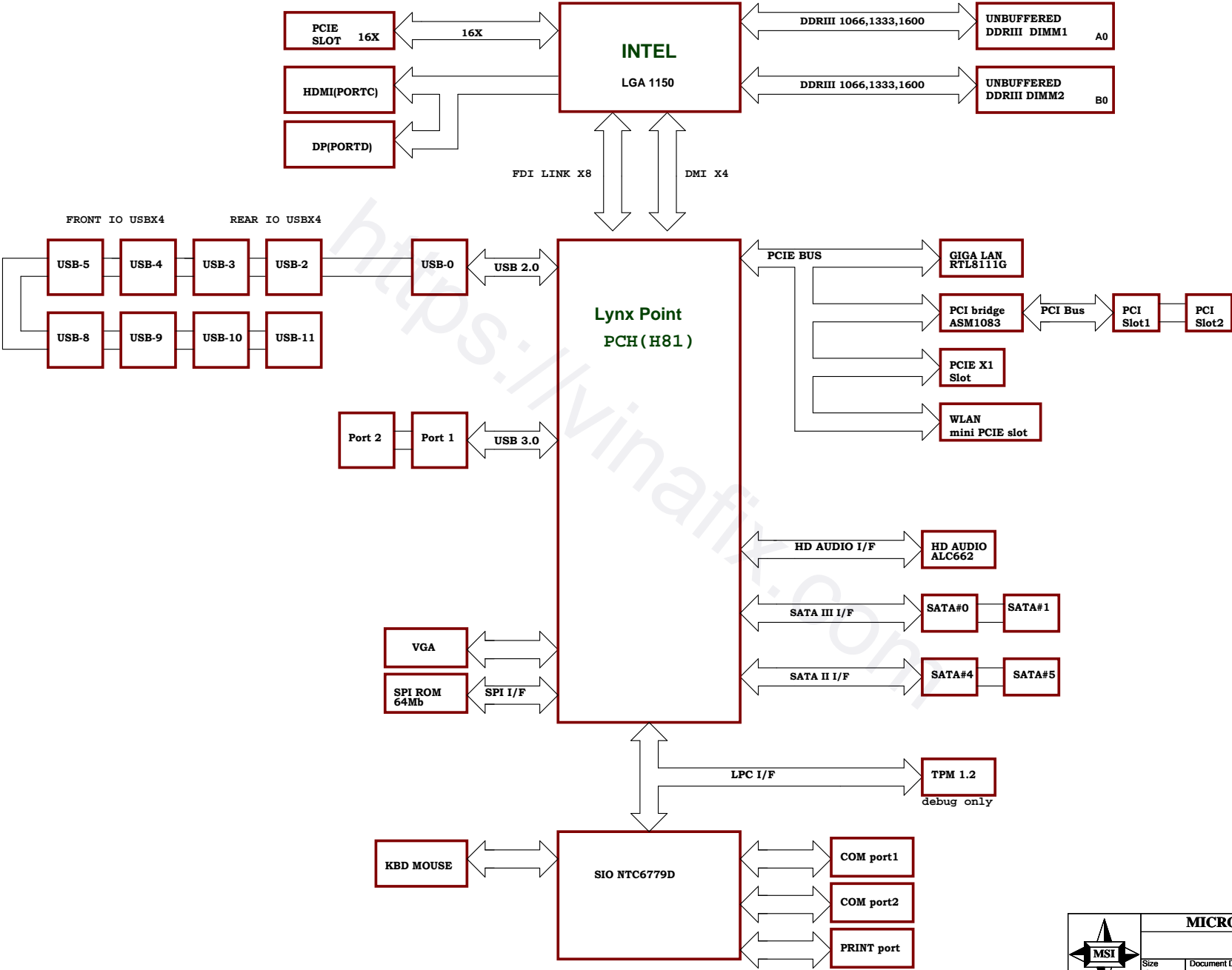
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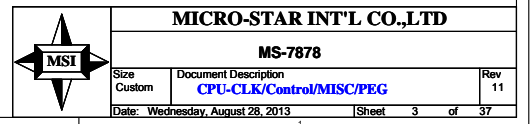


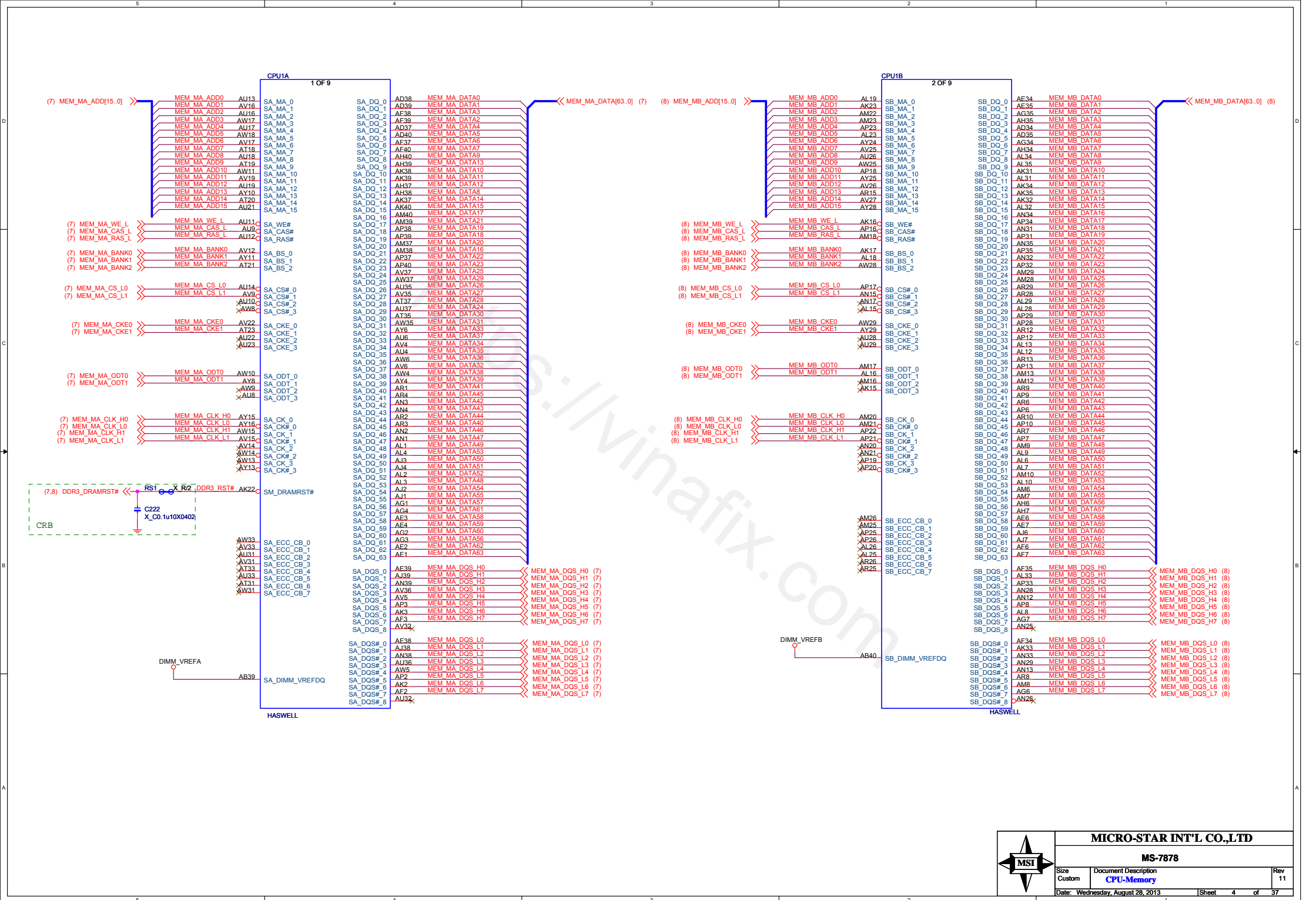
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MS-7878

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Size Custom	Document Description <b>CPU-Power</b>	Rev 11
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GND

GND



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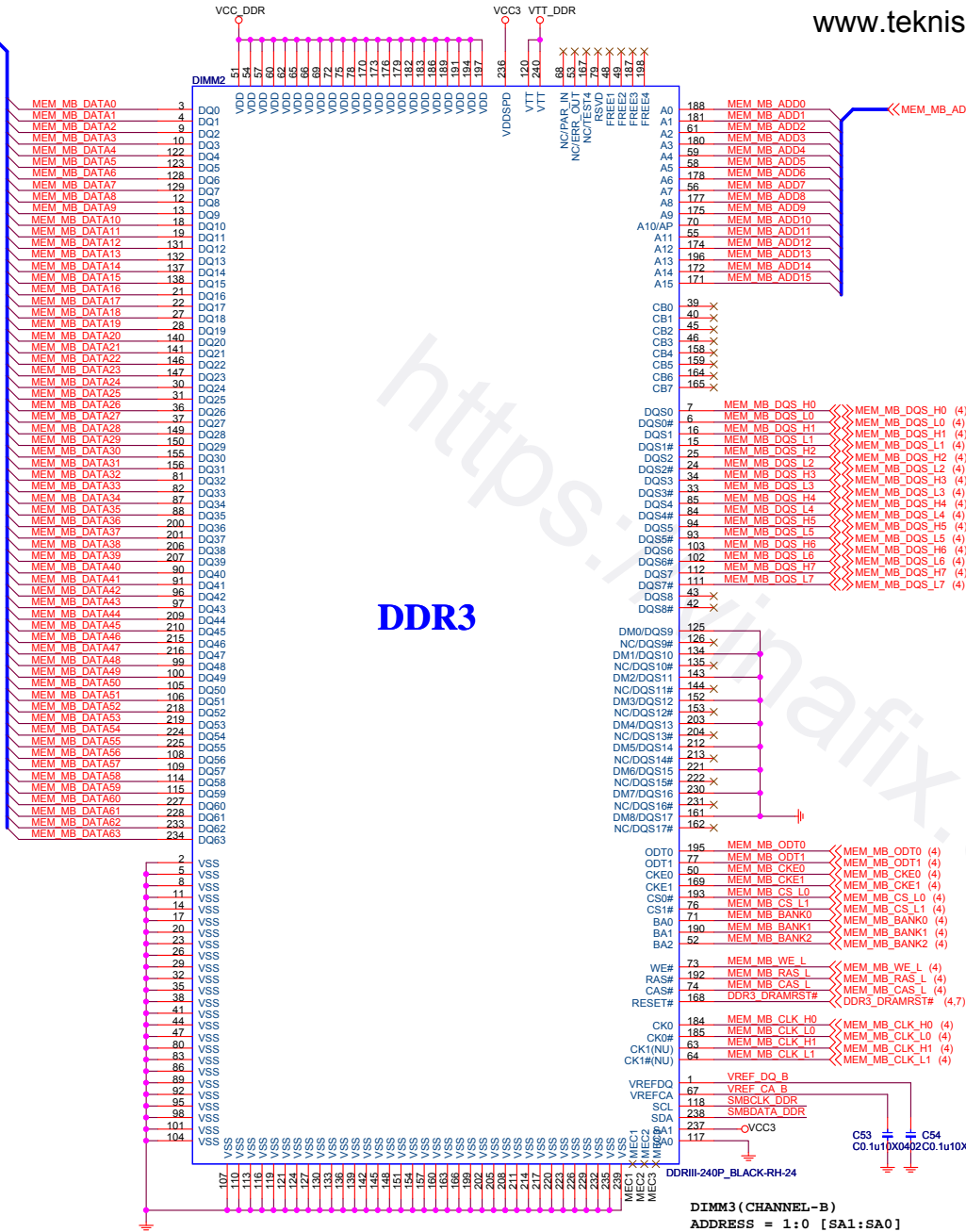




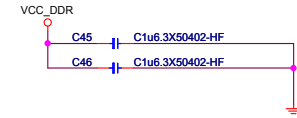
# DDRIII DIMM\_B0

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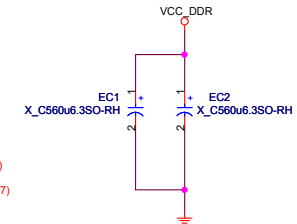
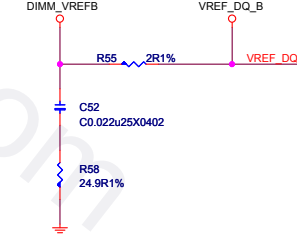
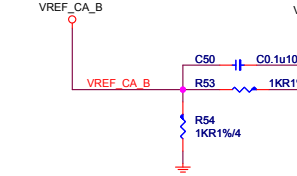
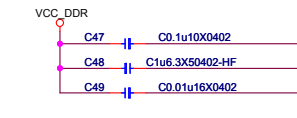
(4) MEM\_MB\_DATA[63..0] <<>



Place close to DIMM2



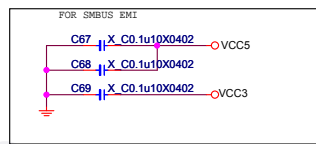
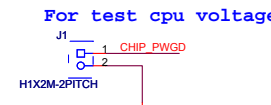
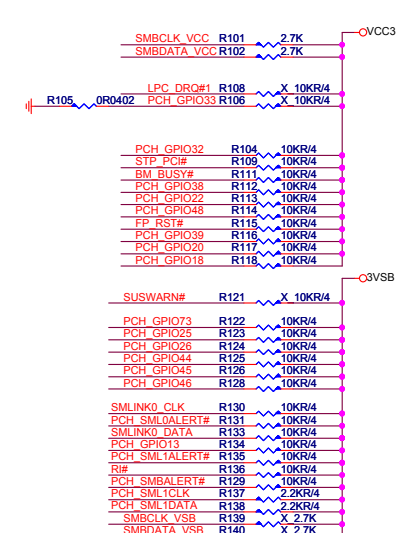
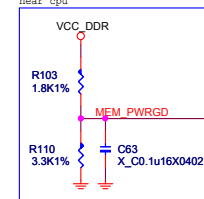
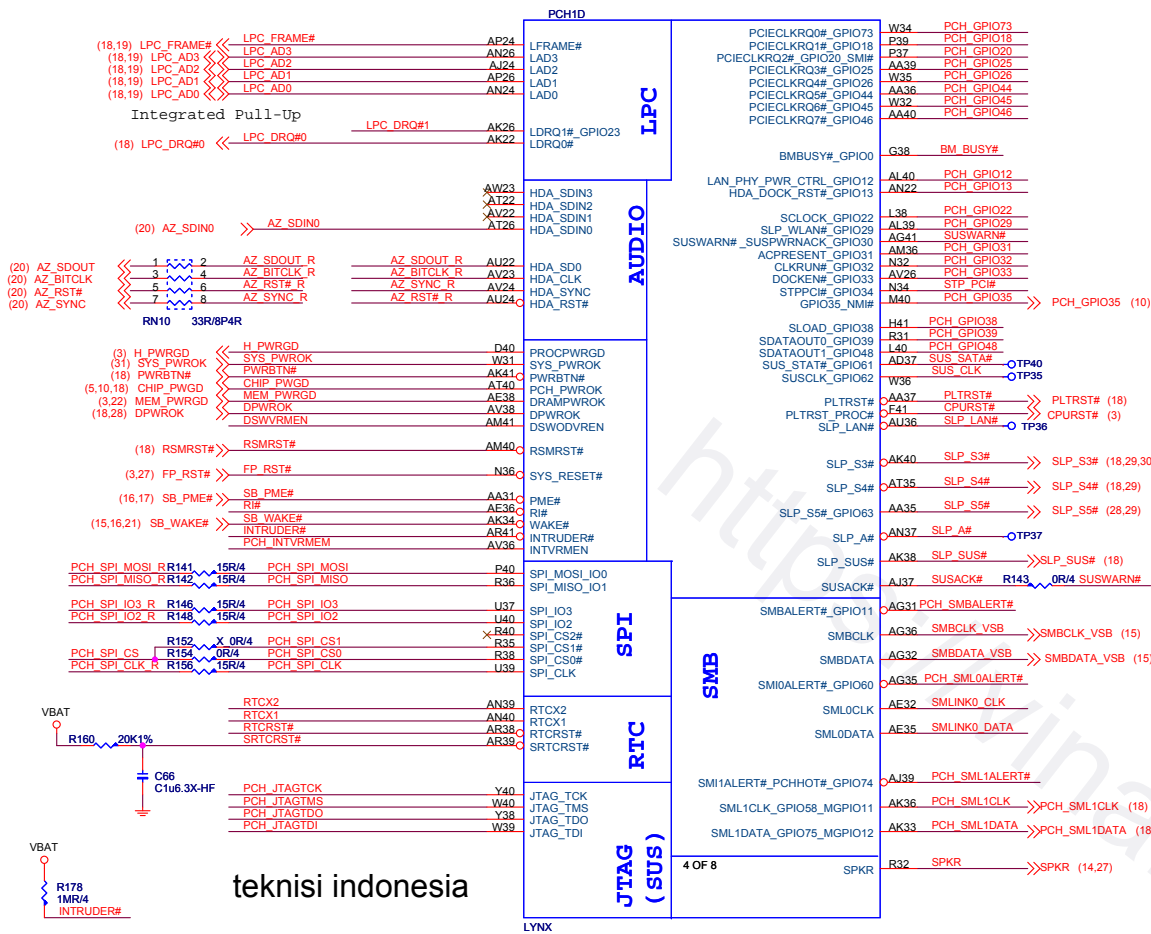
Place close to DIMM2







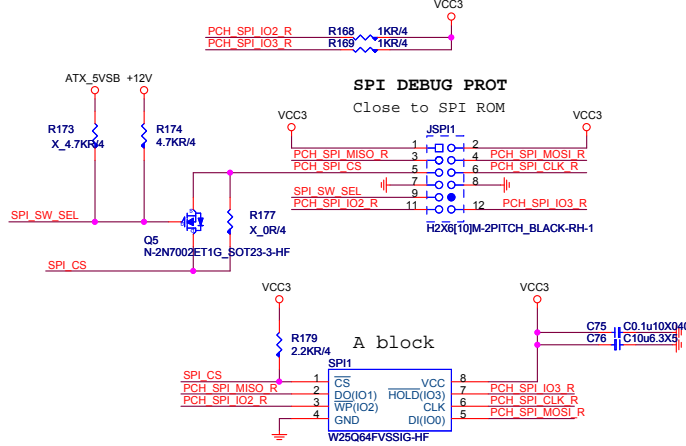
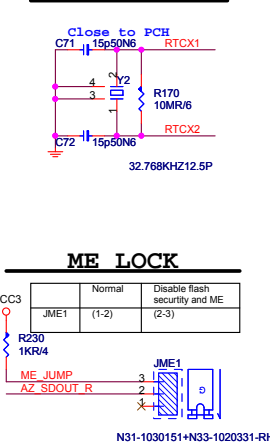




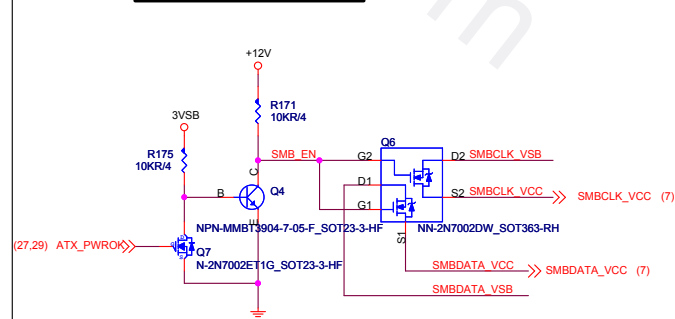
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## SPI ROM

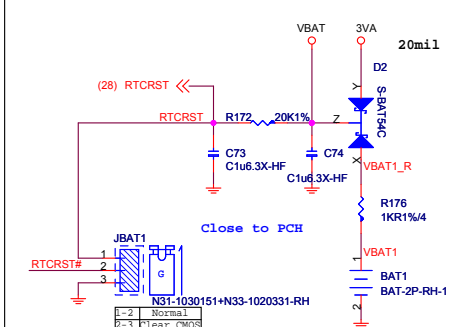
## RTC Block



## SMB Isolation

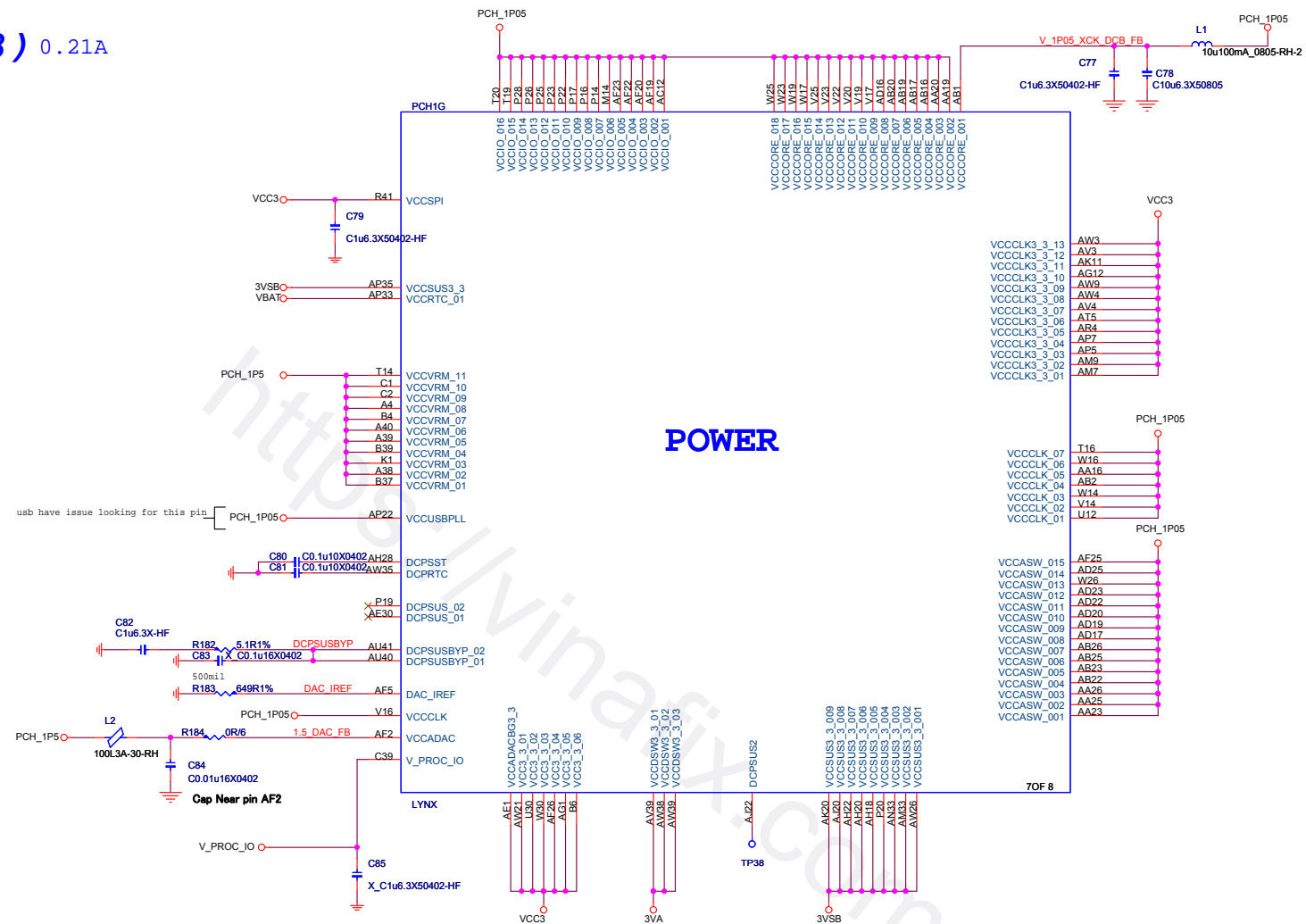


## RTC and CLR\_CMOS

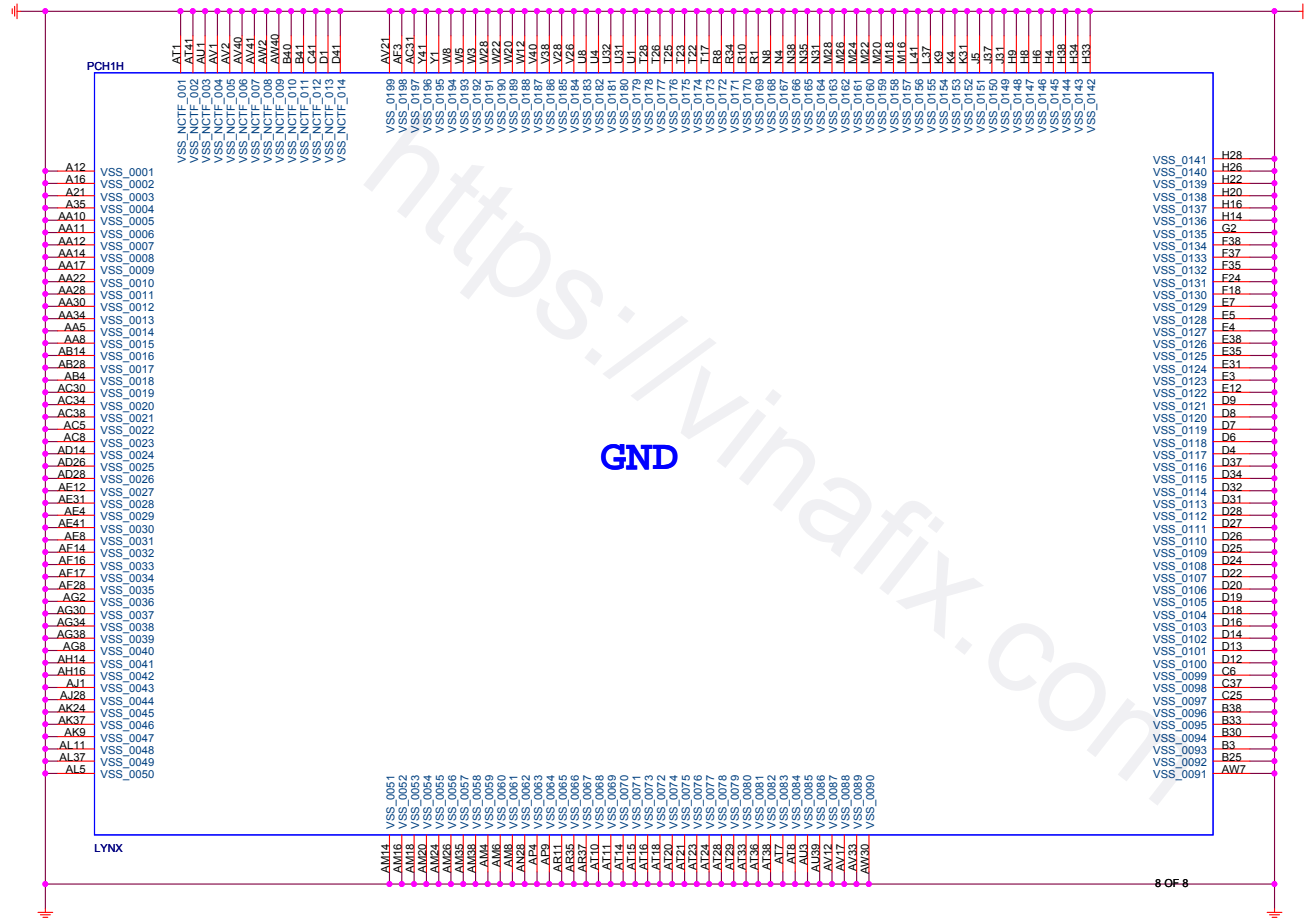


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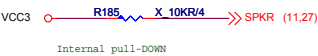
**PCH\_1P05** 5.747A



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PCH Straps

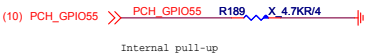


SPKR

Default Mode:

Internal weak Pull-down.

No Reboot Mode with TCO Disabled:  
Connect to Vcc3\_3 with 8.2k-10k Ohm weak pullup resistor.

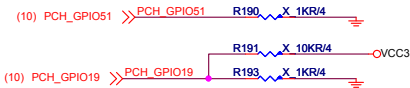


GPIO55

Default Mode:

Internal pull-up.

Top Block Swap Mode:  
Connect to ground with 4.7k Ohm weak pulldown resistor.



SATA1GF/GPIO19, GPIO51

Default (SPI):

Left both SATA1GF/GPIO19 and GPIO51 floating.  
No pull up required.

Boot from PCI:

Connect SATA1GF/GPIO19 to ground with 1k Ohm pull-down resistor.  
Leave GPIO51 Floating.

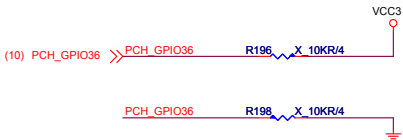
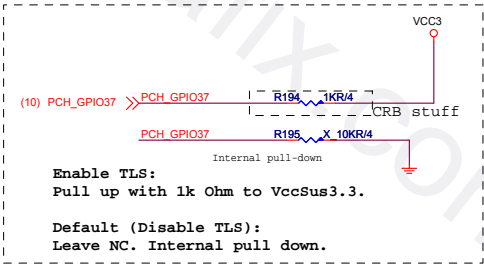
Boot from LPC:

Connect both SATA1GF/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.



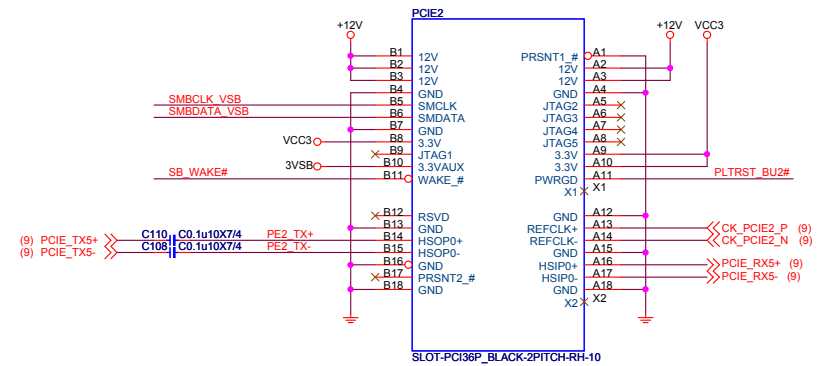
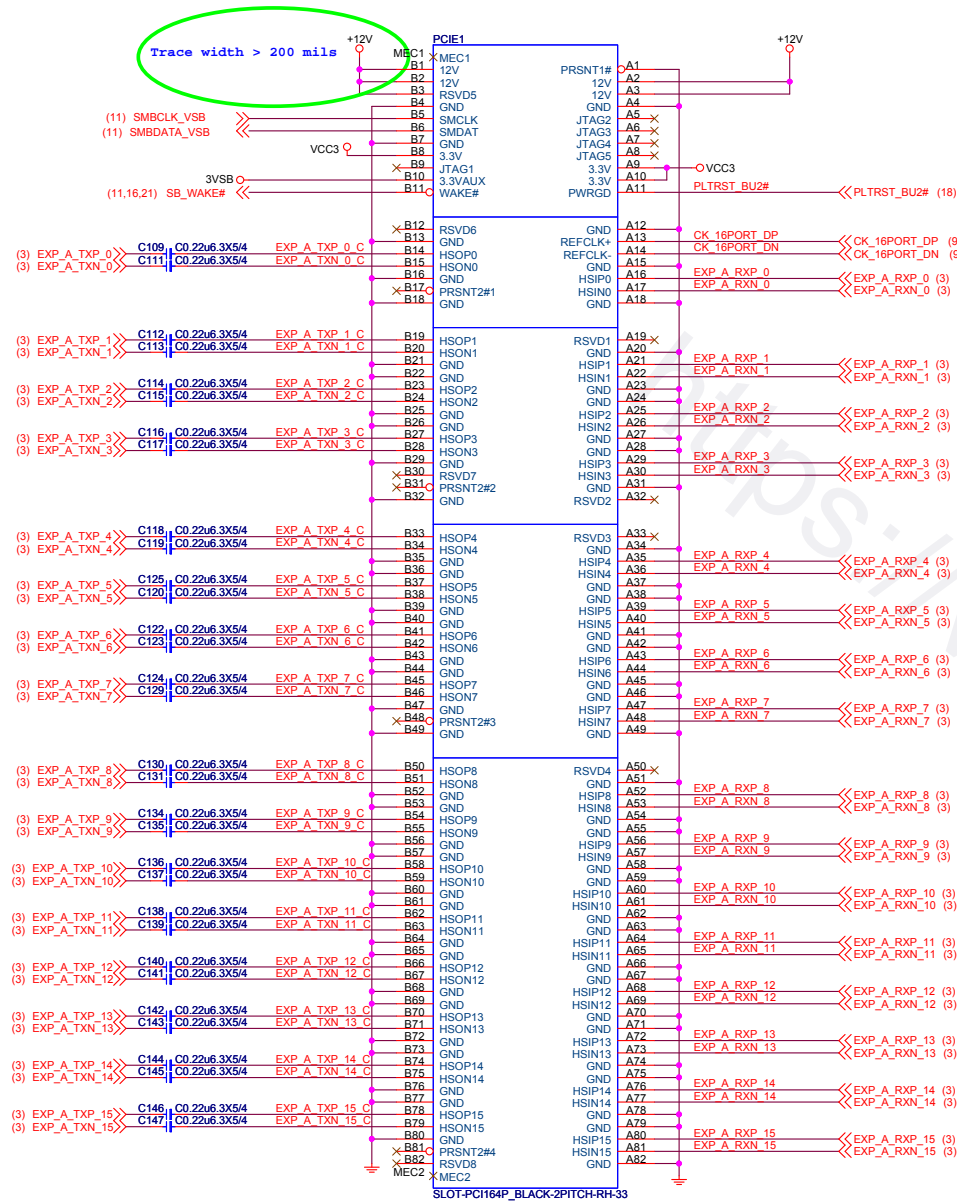
GPIO53

Do not pull low.  
Connect to ground with 1k Ohm pull-down resistor.



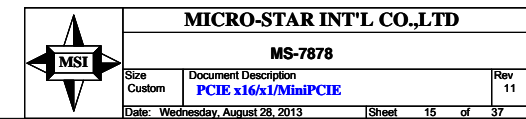
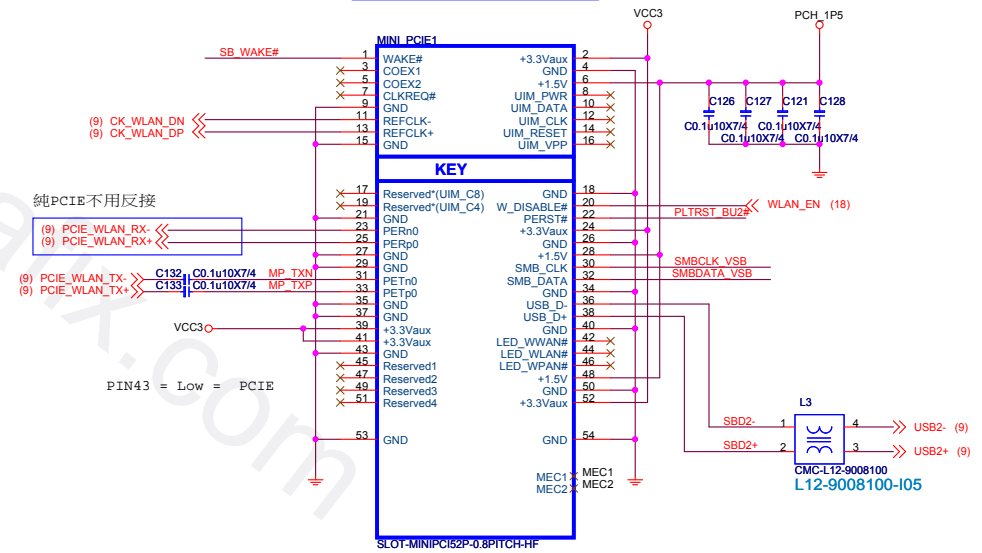
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PCI\_Express X16 slot

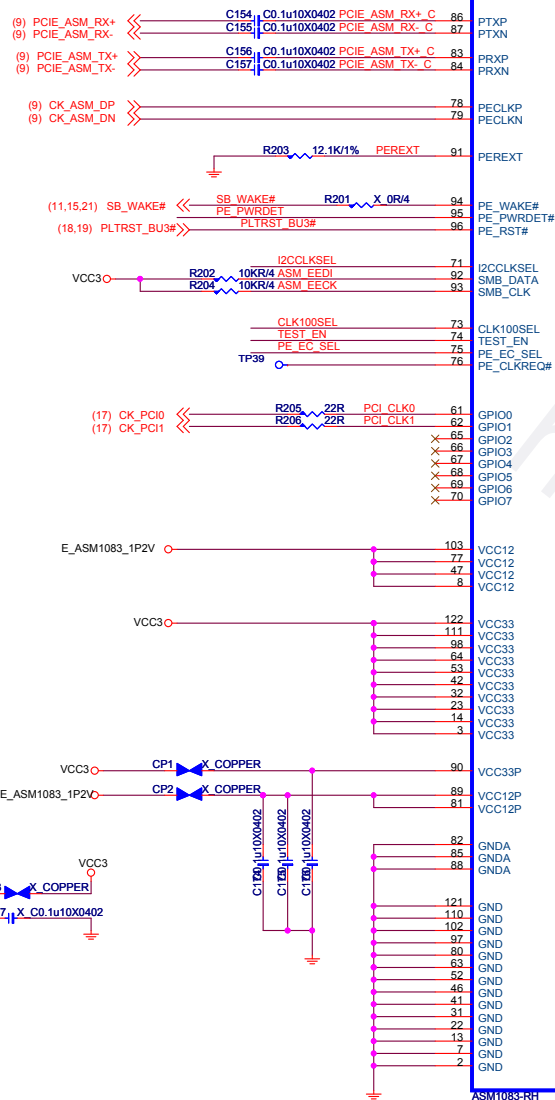


## WLAN

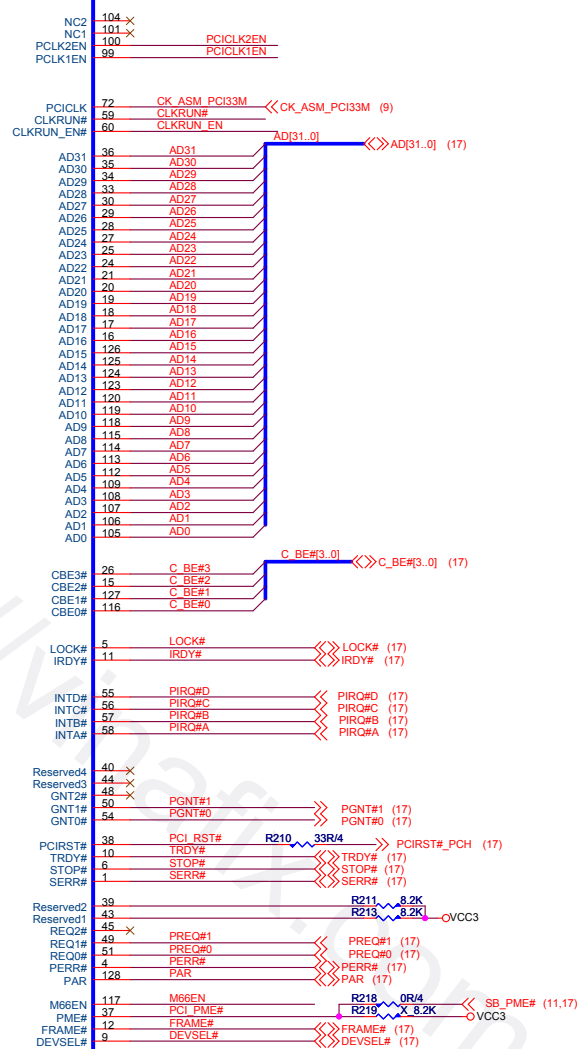
VCC3\_Mini PCIe, 3A







**ASM1083**



## H/W Strapping

PE\_EC\_SEL-  
 "H" for Express Card mode  
 "L" for PCIe Riser Card mode

CLK100SEL-  
 "H" for PECLK input only  
 "L" for PECLK & PCICLK input

TEST\_EN-  
 "H" for Test Mode Enable  
 "L" for Test Mode Disable

CLKRUN\_EN-  
 "H" for CLKRUN Mode Disable  
 "L" for CLKRUN Mode Enable

I2CCLKSEL-  
 "H" is 135KHz I2CCLK  
 "L" is 67.5KHz I2CCLK

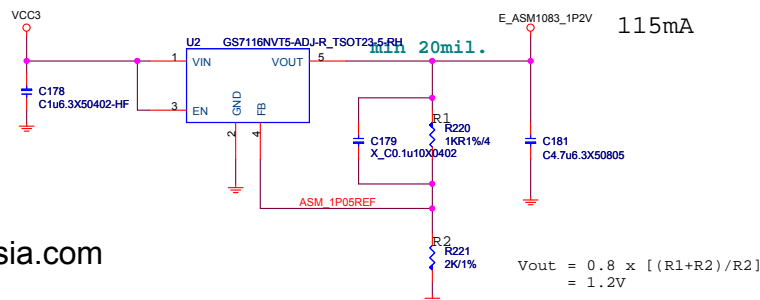


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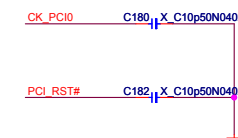
**MS-7878**

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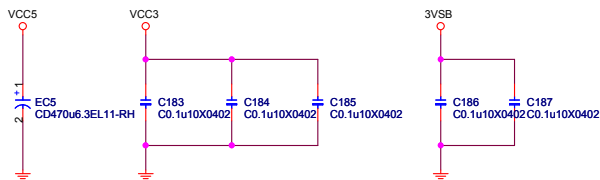
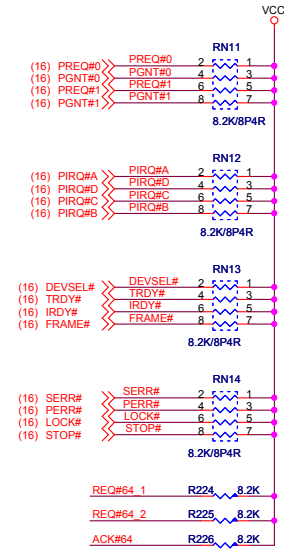
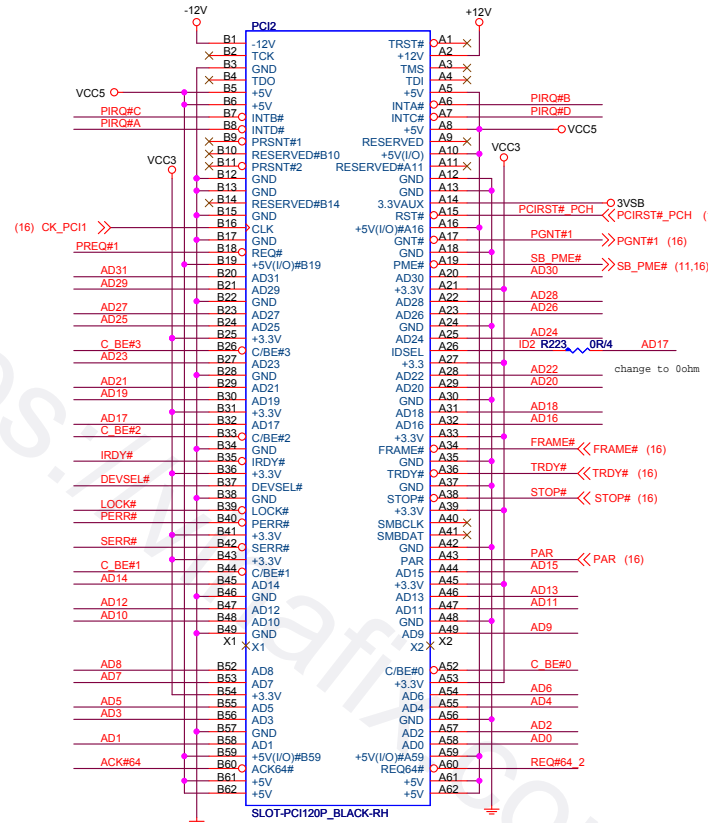
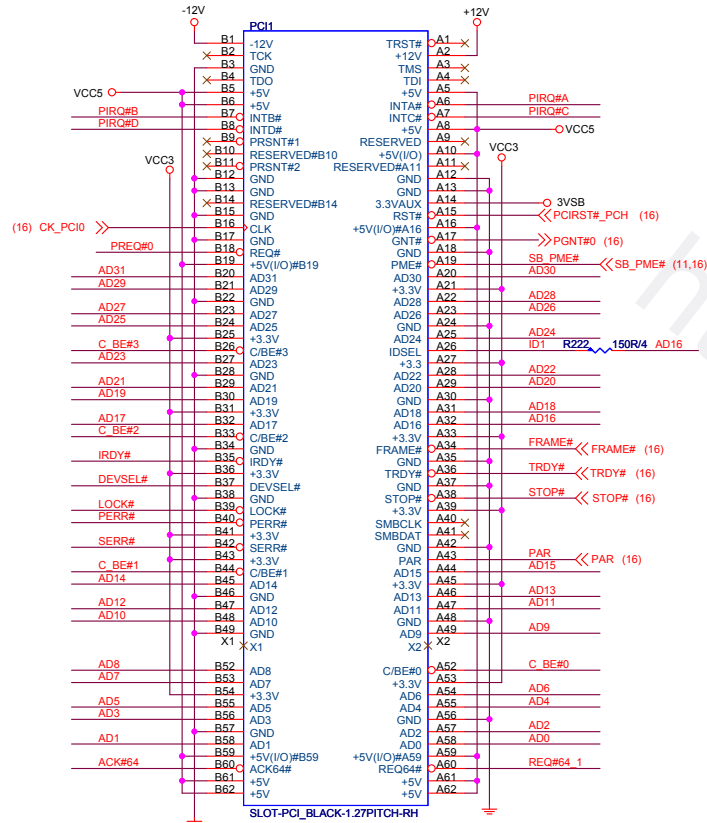
EMI



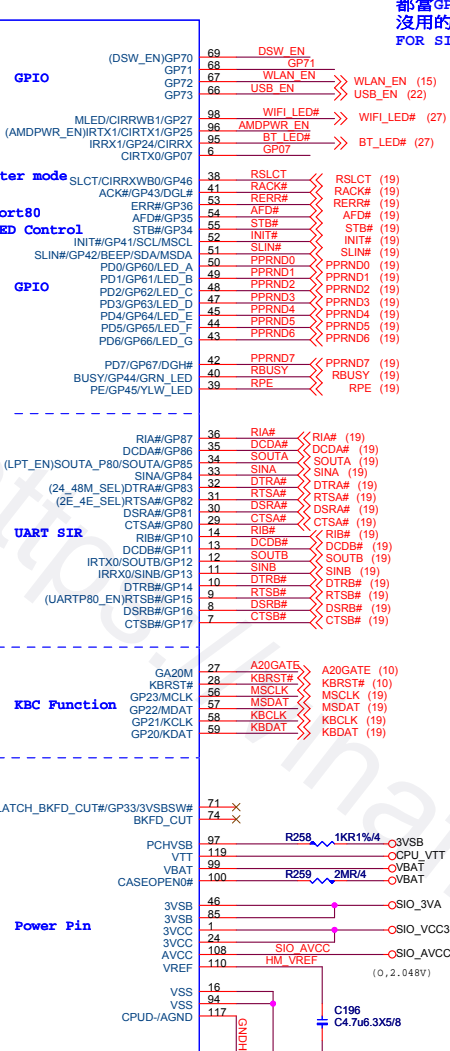
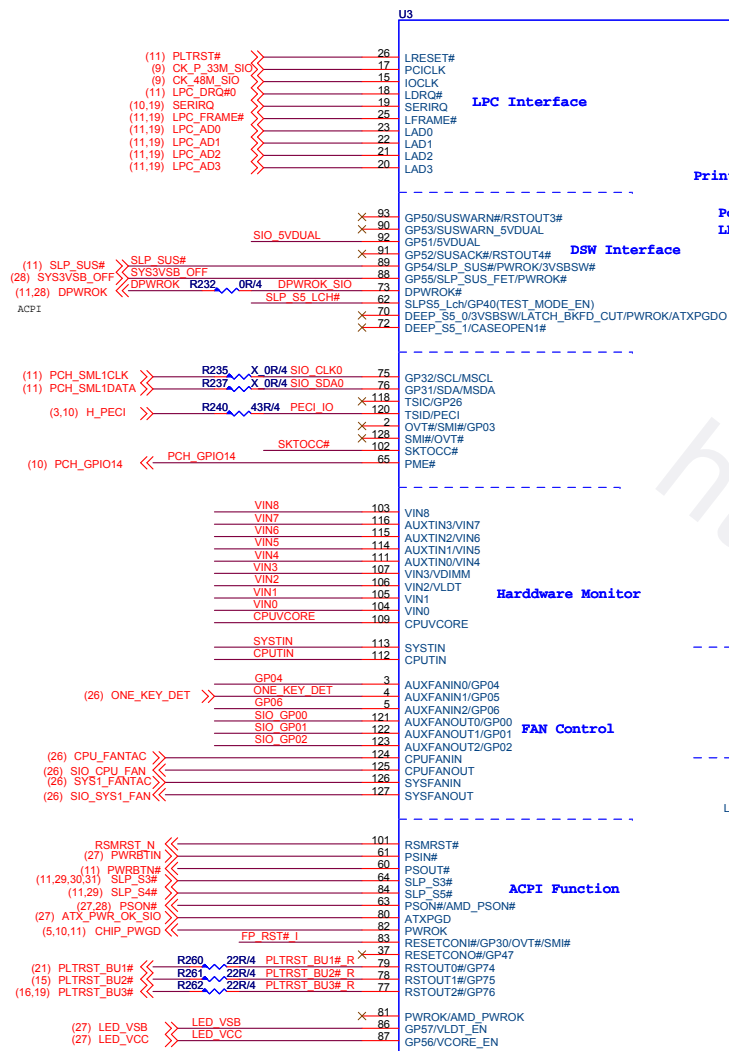
IDSEL = AD16  
MASTER = PREQ#0  
PIRQ#A

IDSEL = AD17  
MASTER = PREQ#1  
PIRQ#B

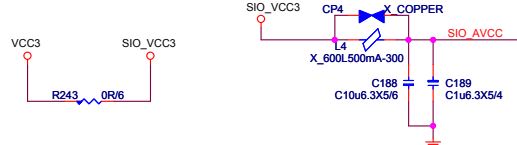
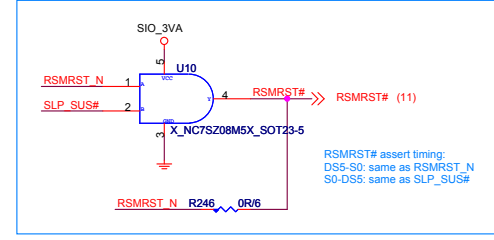
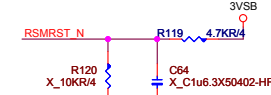
PCI PULL-UP / DOWN RESISTORS



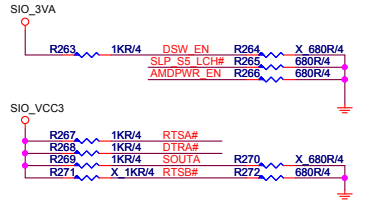
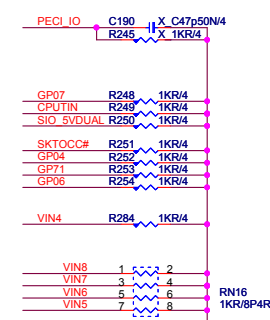
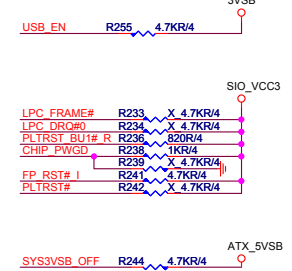
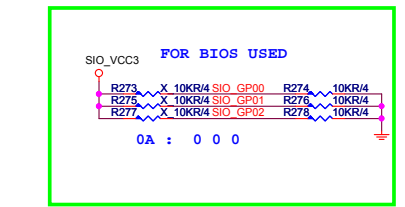
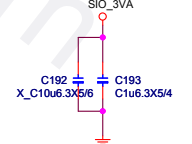
PCI slot (X1)	
+3.3Vaux (wake)	- 1125mA
+3.3Vaux (no wake)	- 60mA
+3.3V	- 7.6A
+5V	- 5A
+12V	- 0.5A



都當GPIO  
沒用的GPIO PIN 請PULL DOWN  
FOR SIO POWER CONSUMPTION



close to pin99

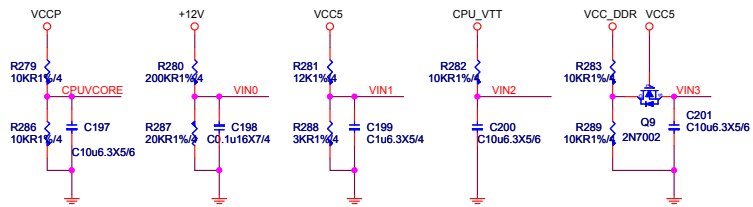


(PIN31)RTSA#	0=2E	1=4E
(PIN32)DTRA#	0=24MHz	1=8MHz
(PIN34)SOUTA	0=Port80 Enable	1=PRT Enable
(PIN69)DSW_EN	0=Disable	1=Enable
(PIN9) (RTSB#)ORT80_EN	0=Disable	1=Enable
(PIN96)AMPDPWR_EN	0=Disable	1=Enable
(PIN62)(SLP_SS_LCH#)TEST_MODE_EN	0=Disable	1=Enable

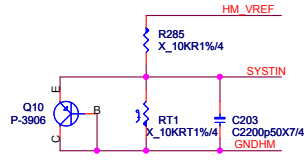
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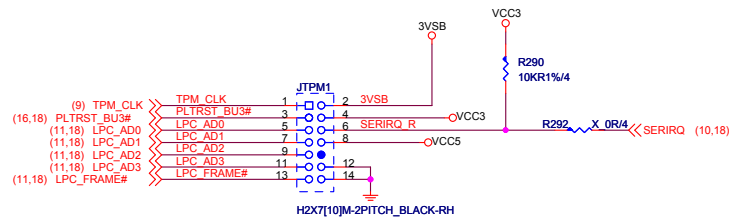
## HW Monitor - Voltage



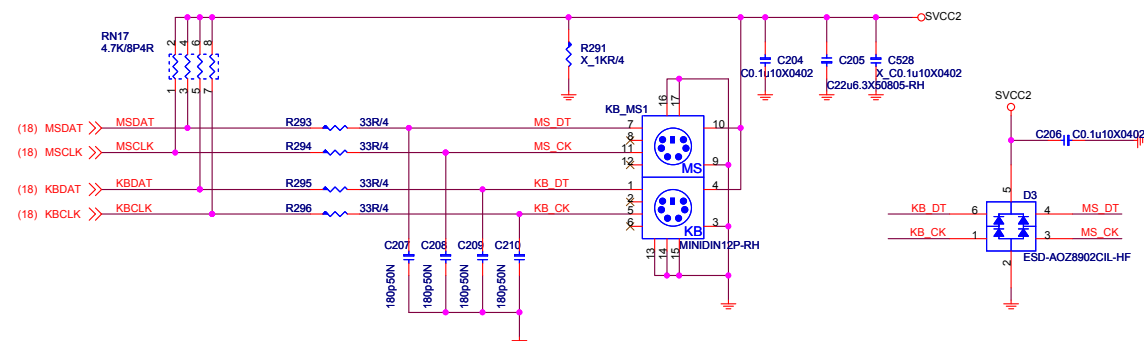
## Thermal Resistor



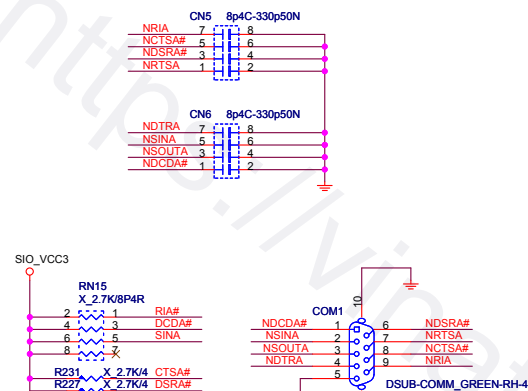
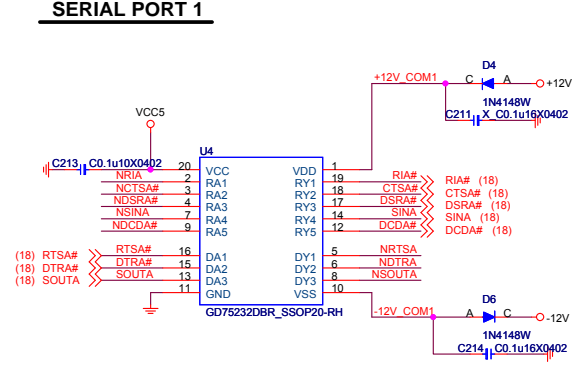
## TPM/JLPC



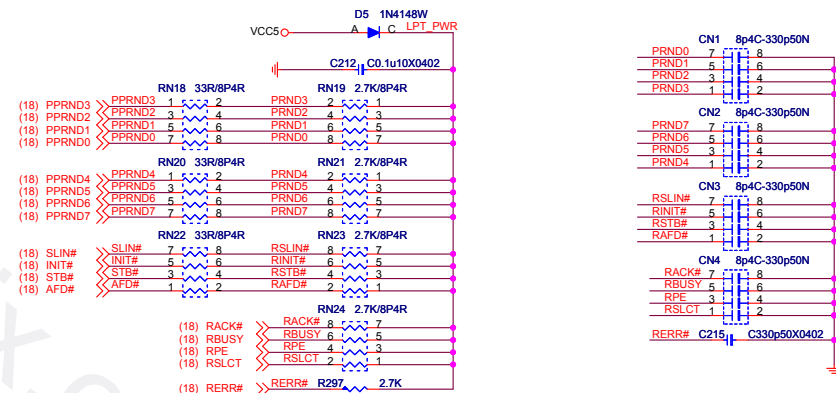
## PS2 KB&amp;MS



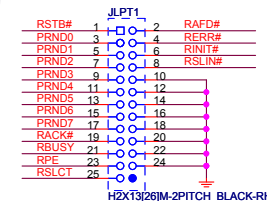
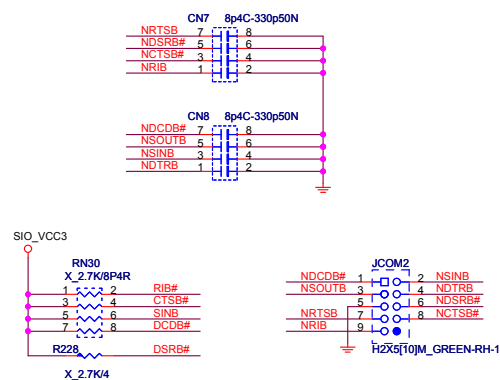
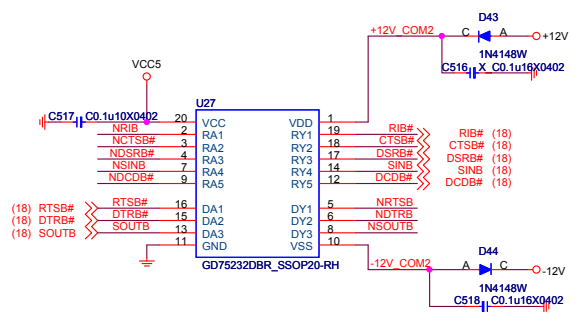
## SERIAL PORT 1



## PARALLAL PORT



## SERIAL PORT 2

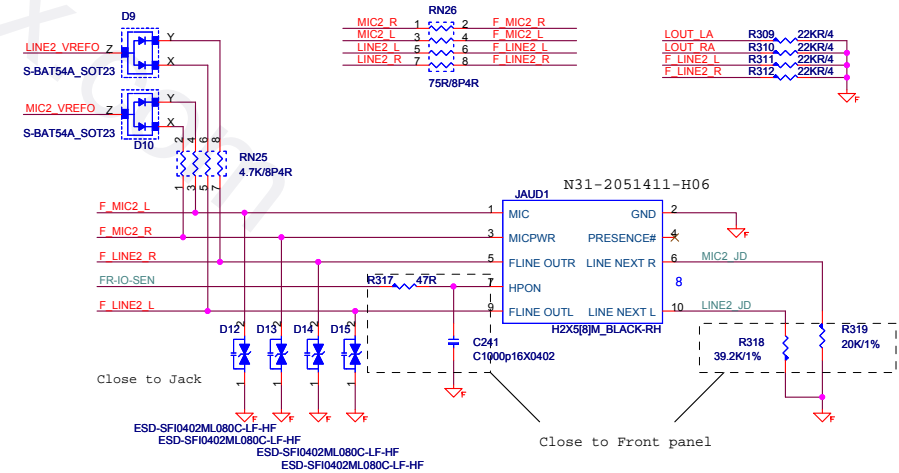
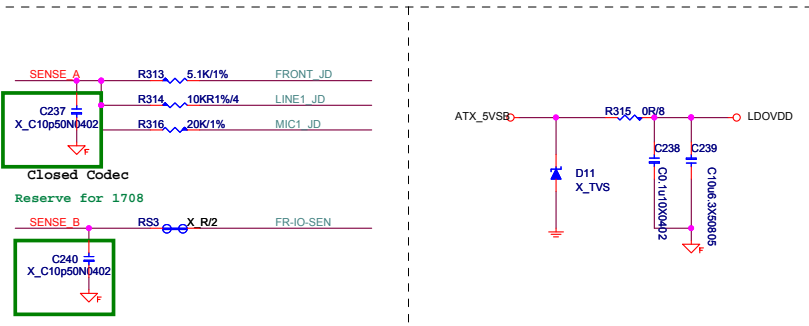
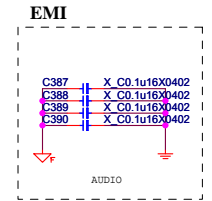
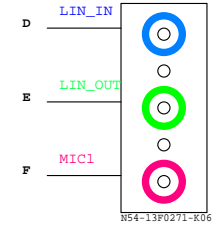
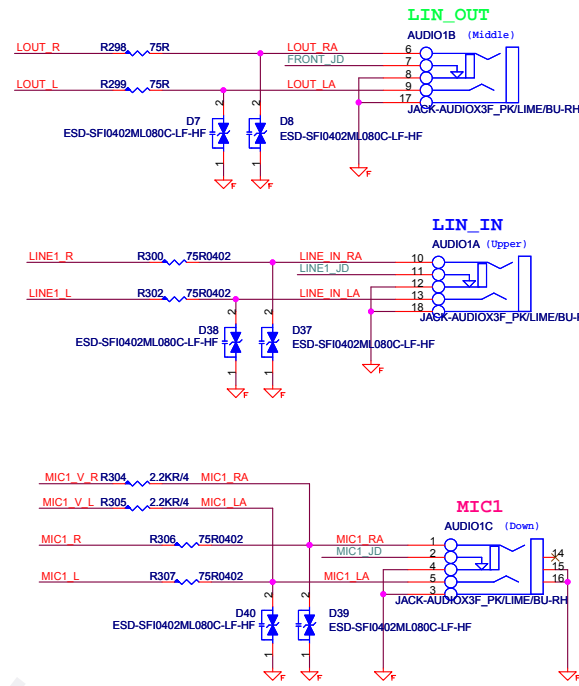
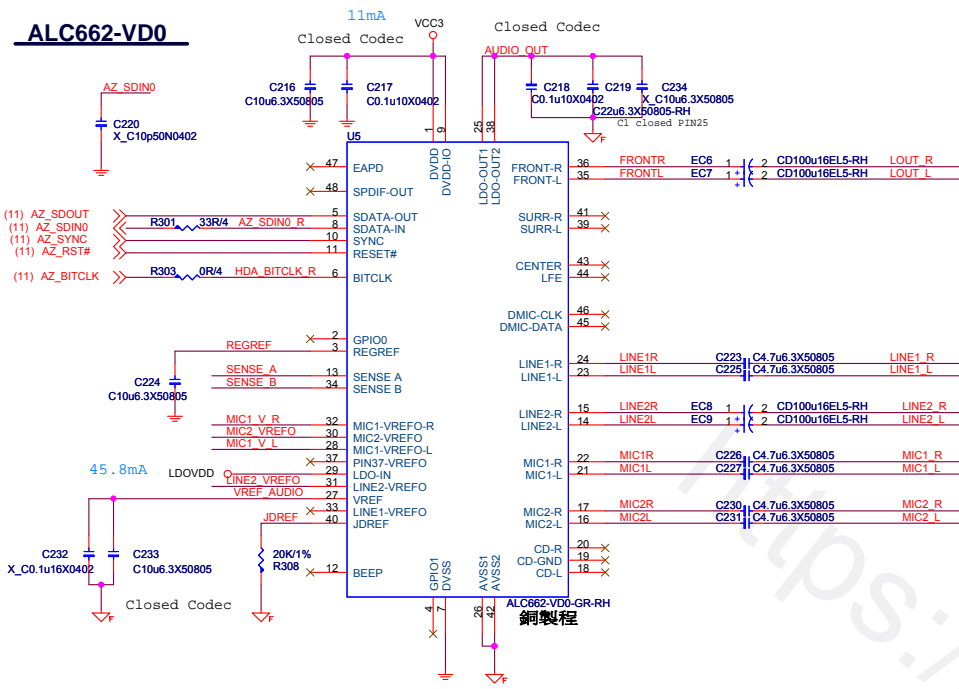


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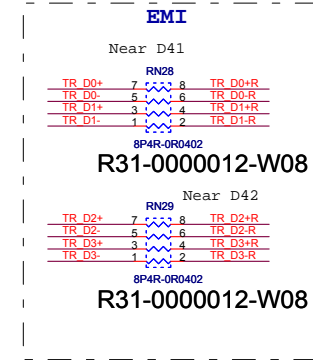
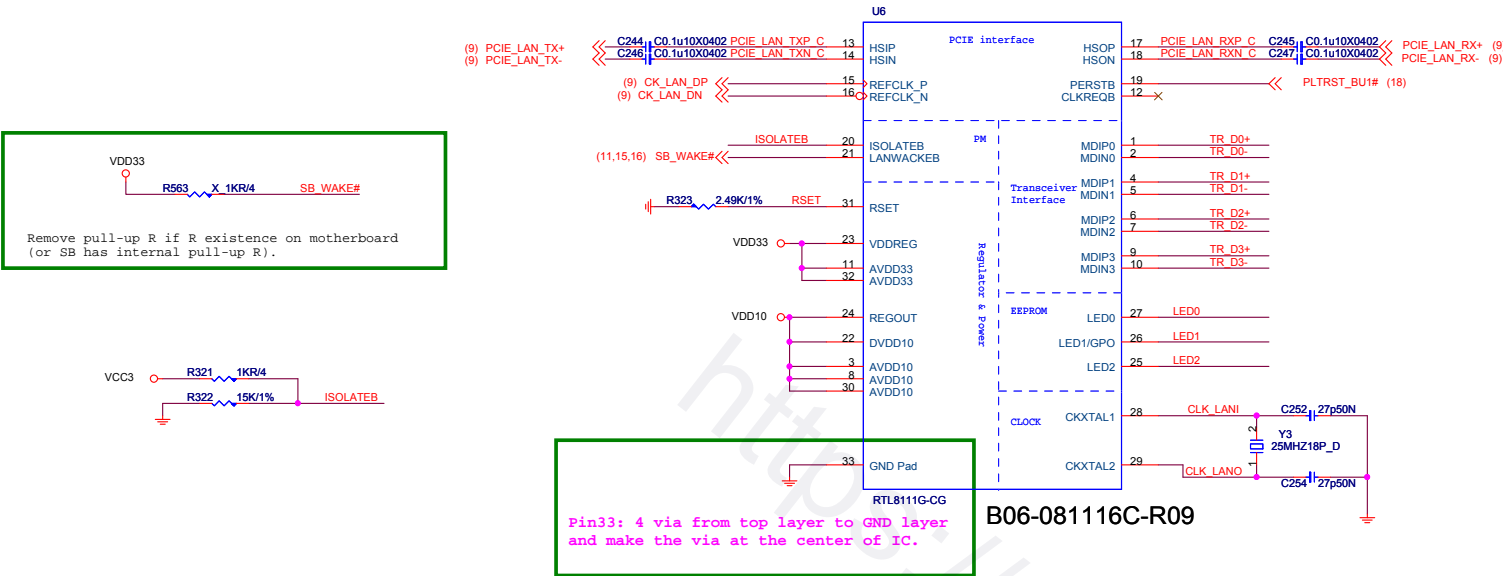
# ALC662-VD0



Varister --> cap for cost down

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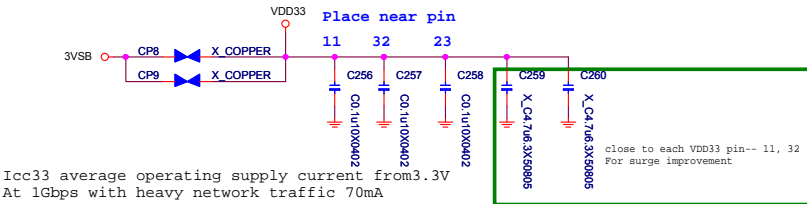
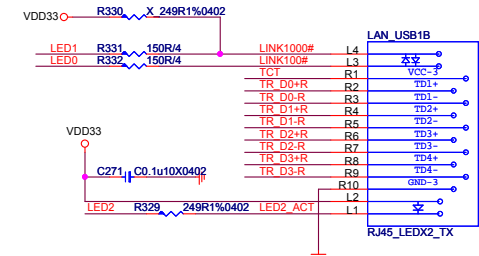
# RTL8111G Giga LAN



## LAN Connector

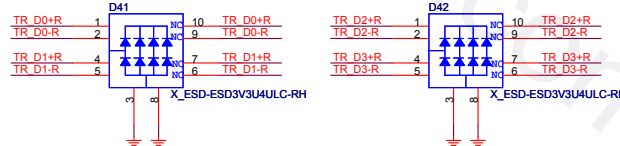
8111G: Keep RL6 and Remove RL5 for RTL8111G

Support R= 249 ohm Resistor For Single Color LED.  
Support R= 125 ohm Resistor For Dual Color LED.



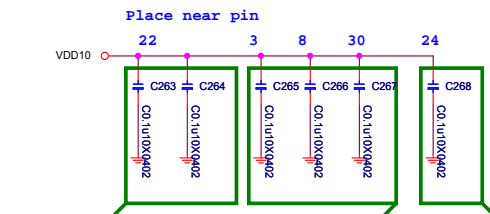
## Reserve ESD Protect

ESD PIN1 Near Connector Side



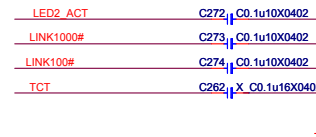
D0G-05A0300-I14

D0G-05A0300-I14



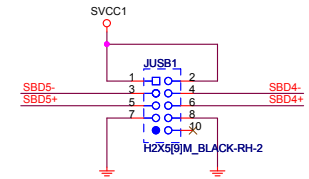
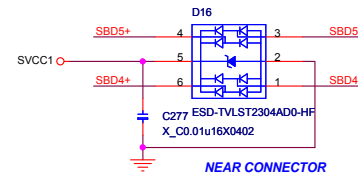
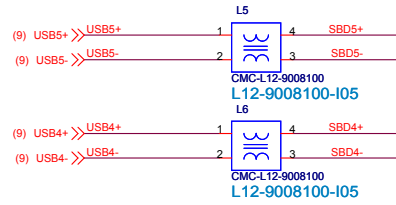
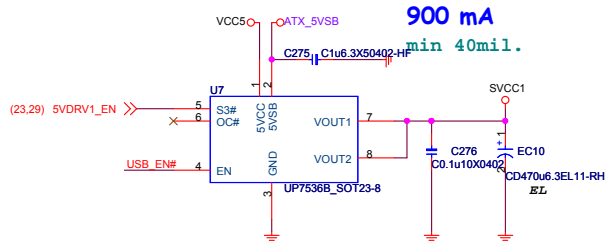
8111G: close to pin 22 8111G: close to pin 3,8,30 8111G: LDO mode close to pin 24

Icc10 average operating supply current from 1.0V  
At 1Gbps with heavy network traffic 300mA

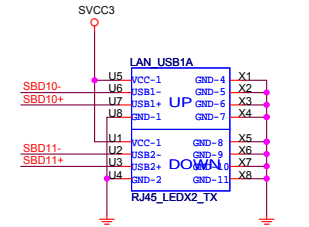
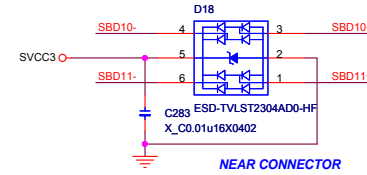
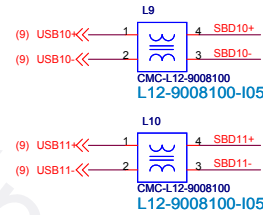
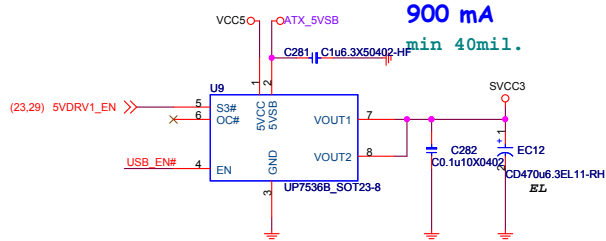


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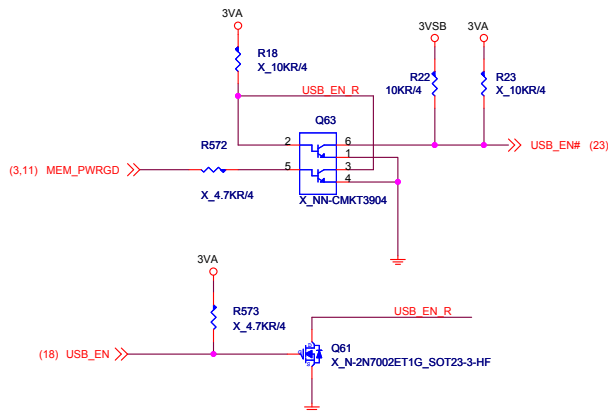
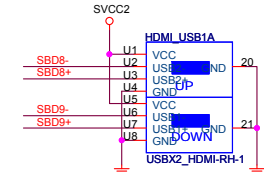
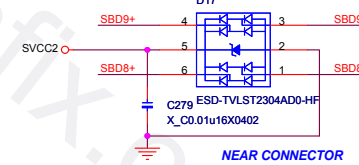
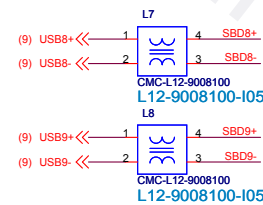
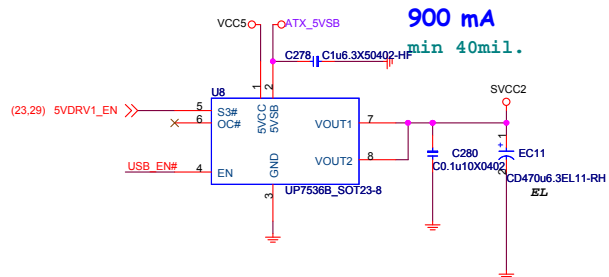
### FRONT USB PORT 4,5



### REAR USB PORT 10,11



### REAR USB PORT 8,9



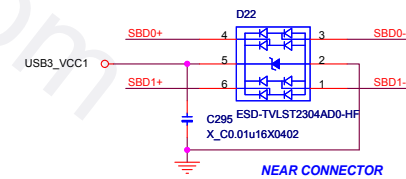
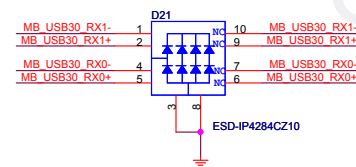
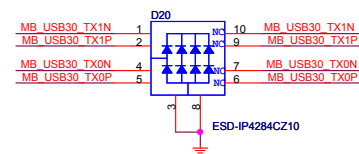
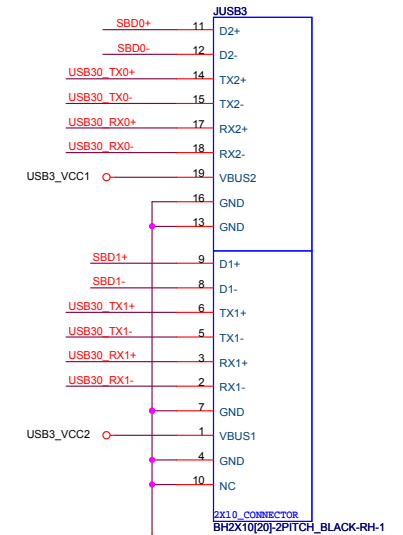
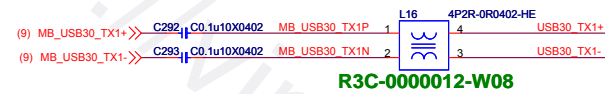
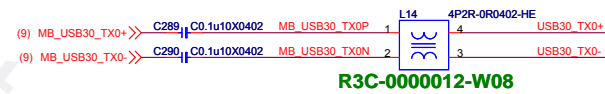
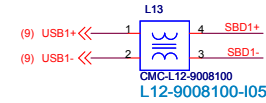
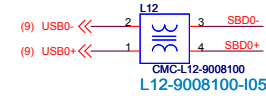
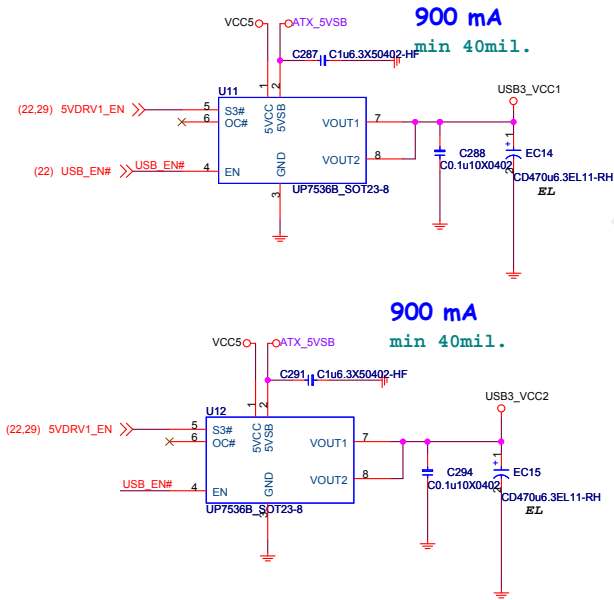
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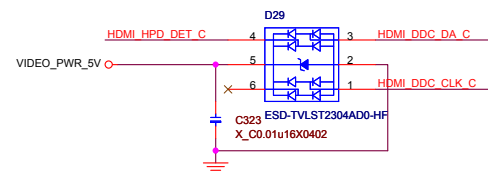
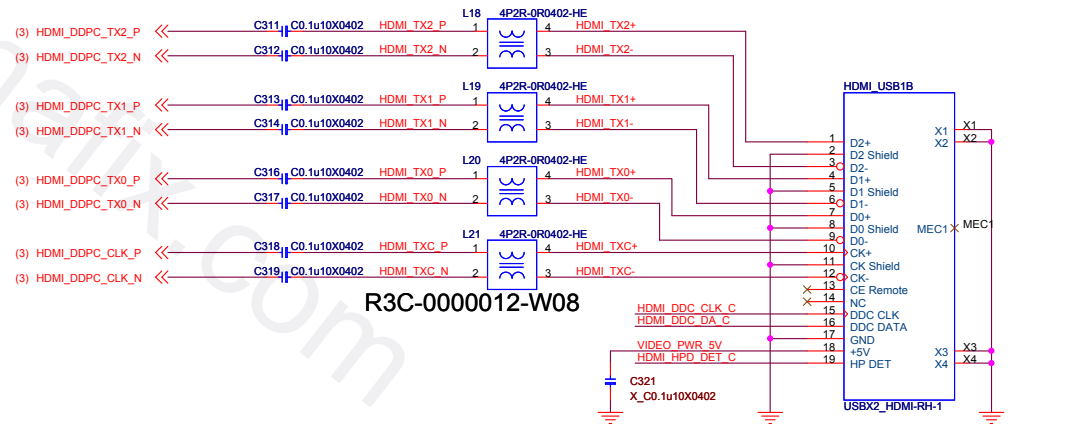
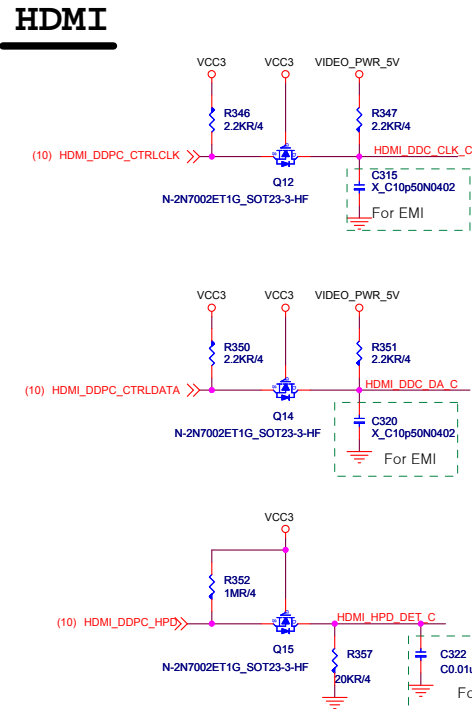
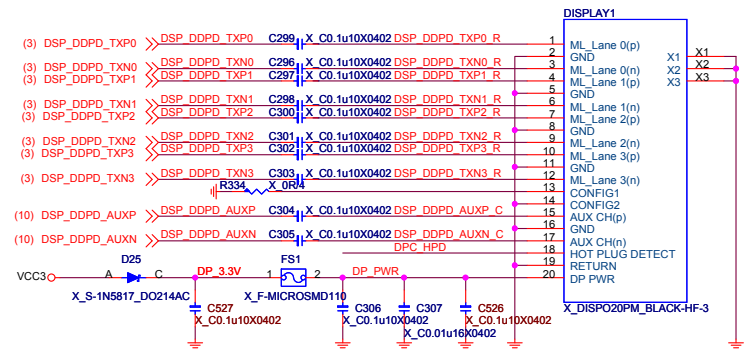
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# FRONT USB3.0 PORT1.2 & USB2.0 PORT 2,3



The schematic diagram illustrates the DDPD HPD driver circuit. It features two input signals, (10) DSP\_DDPD\_HPDI and (11) DSP\_DDPD\_HPDI, which are connected to the non-inverting inputs of a differential pair of NMOS transistors, Q11 and Q12. The gates of Q11 and Q12 are connected to VCC3 and VCC5, respectively. The sources of Q11 and Q12 are connected to ground. The drains of Q11 and Q12 are connected to VCC3 and VCC5, respectively. The output of Q11 is connected to the DDPD\_HPDI signal line through a resistor R338. The output of Q12 is connected to the DDPD\_HPDI signal line through a resistor R339. The DDPD\_HPDI signal line is also connected to the DDPD\_HPDI signal line through a resistor R338. The DDPD\_HPDI signal line is connected to the DDPD\_HPDI signal line through a resistor R339. The DDPD\_HPDI signal line is connected to the DDPD\_HPDI signal line through a resistor R338. The DDPD\_HPDI signal line is connected to the DDPD\_HPDI signal line through a resistor R339.



HDMI TX2-	R353	510R0402	HDMI TX2+
HDMI TX1-	R354	510R0402	HDMI TX1+
HDMI TX0-	R355	510R0402	HDMI TX0+
HDMI TXC-	R356	180R0402-RH	HDMI TXC+

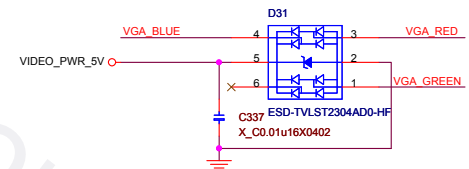
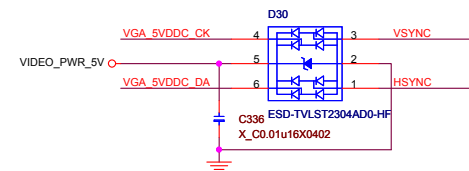
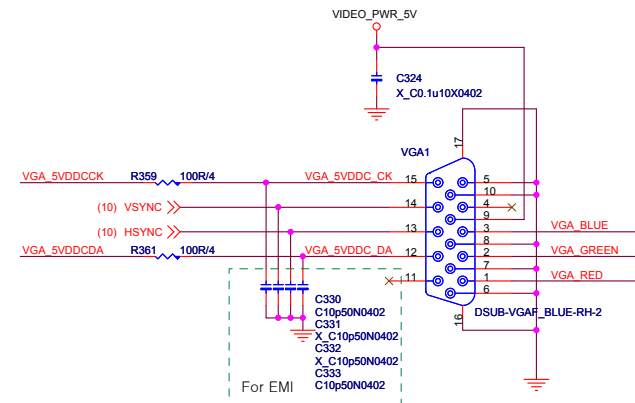
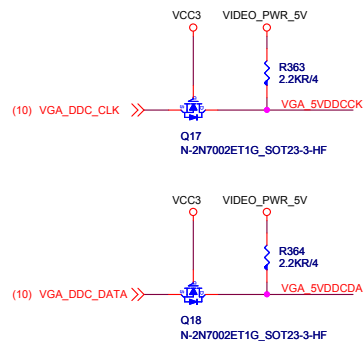
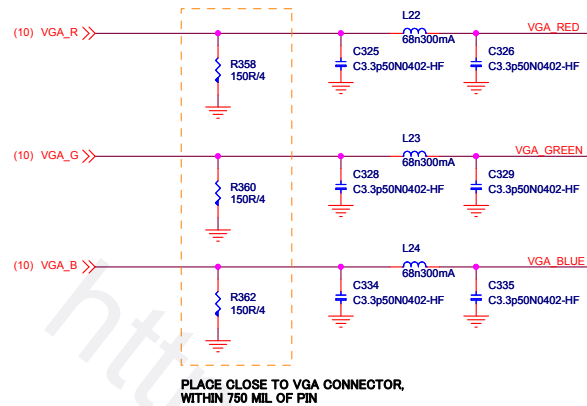
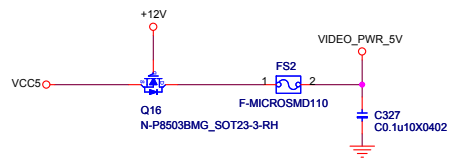
HDMI bridge for EMI



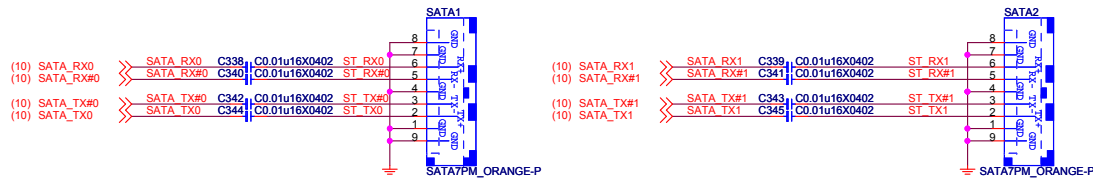
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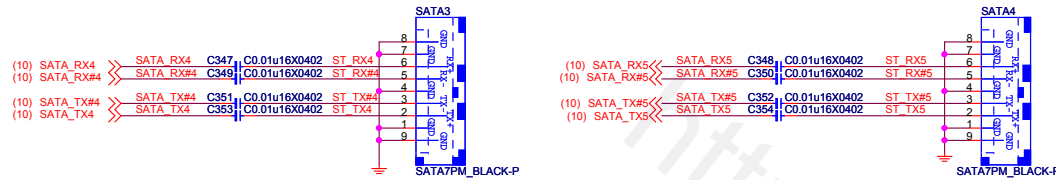
# VGA



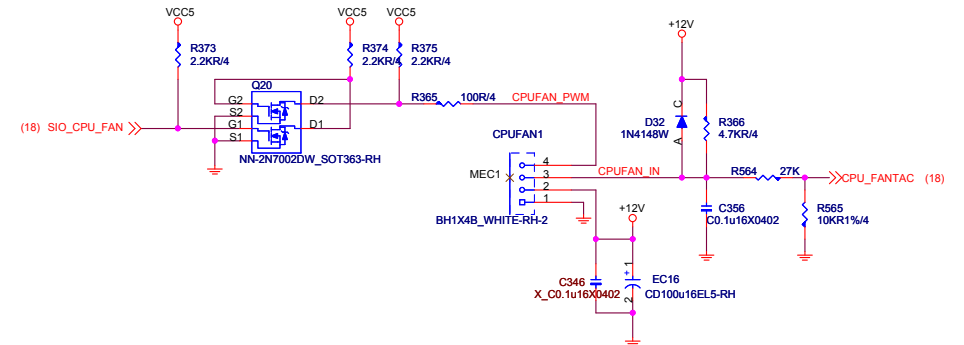
## SATA 6G PORT 0,1



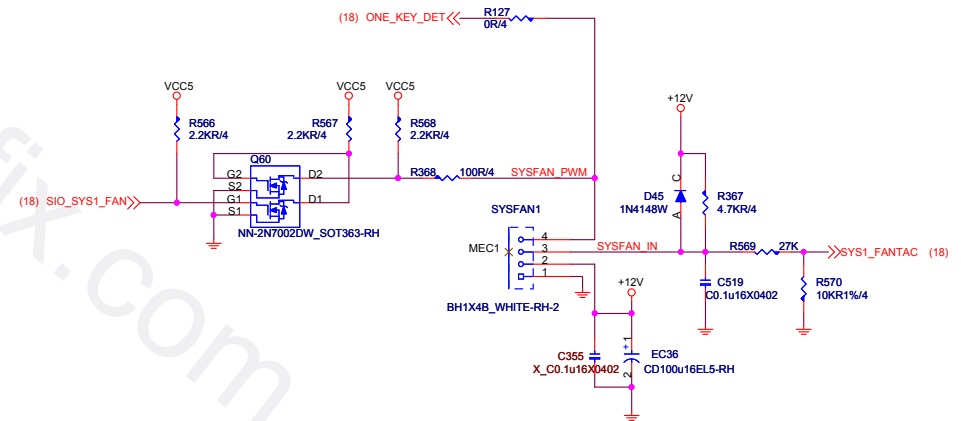
## SATA 3G PORT 4,5



## CPU FAN-COUNTROL CIRCUIT



## SYS FAN-COUNTROL CIRCUIT

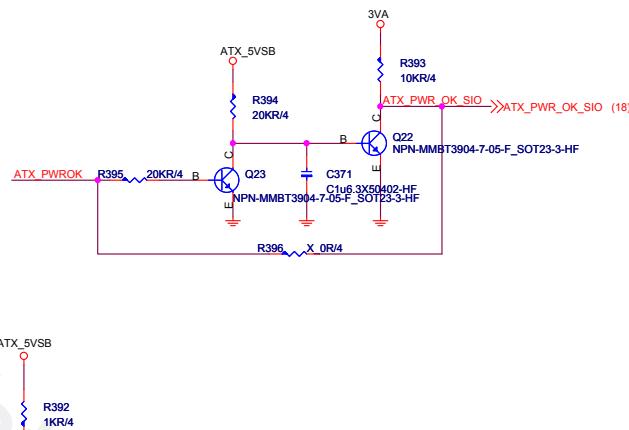
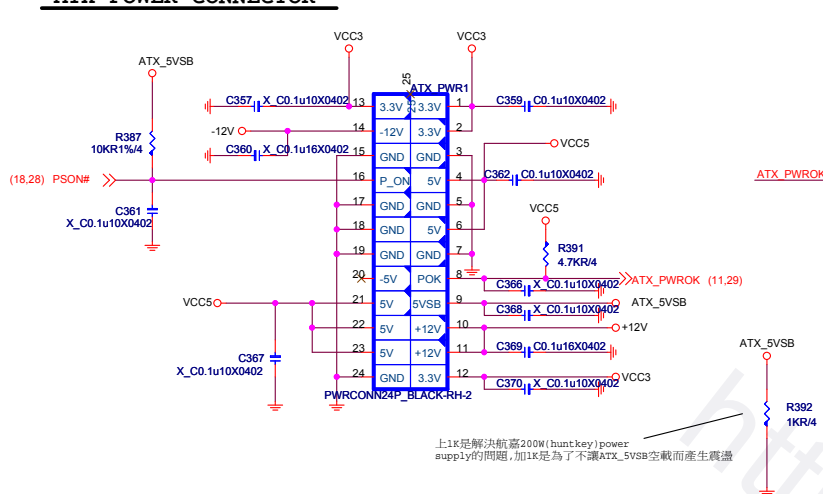


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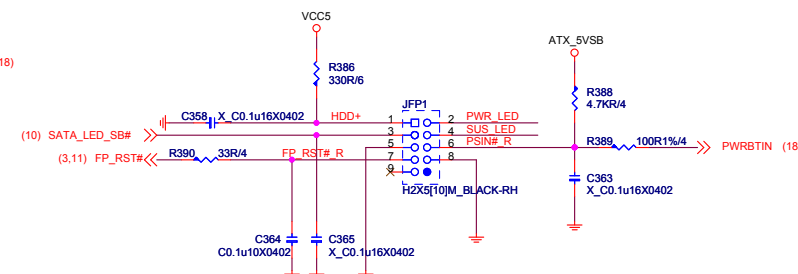
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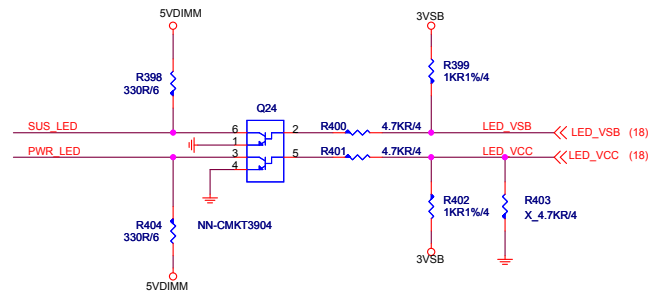
## ATX POWER CONNECTOR



## FRONT PANNEL

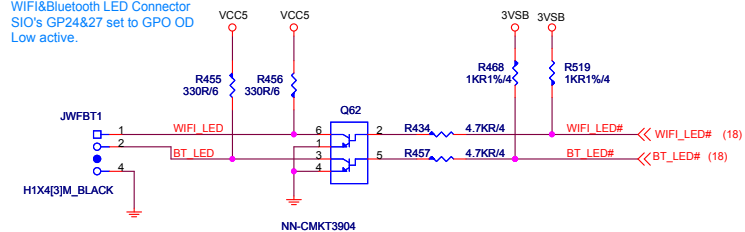


## Power & Suspend LED



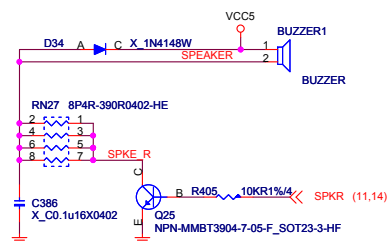
## WIFI & BT LED

WIFI&Bluetooth LED Connector  
SIO's GP24&27 set to GPO OD  
Low active.

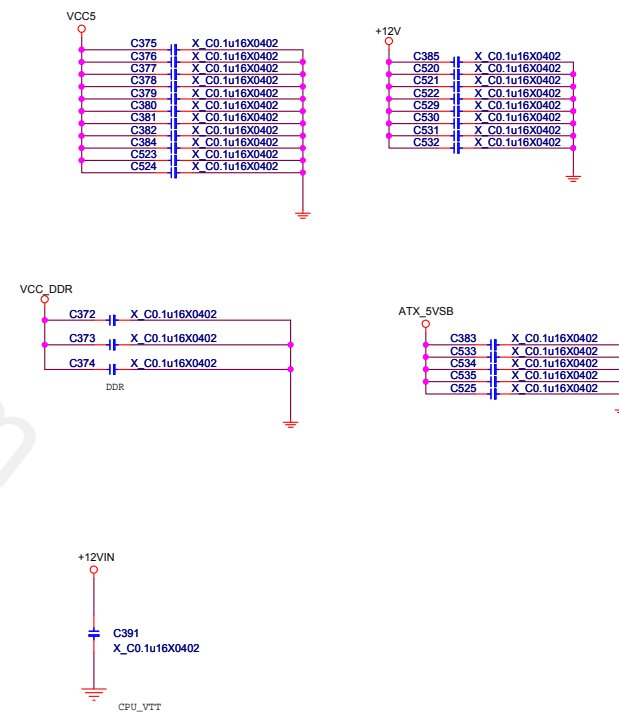


## Buzzer

R=390 Ohm  
I=(5-0.2)/R=0.0123 A  
W=0.0123A x 5v=0.0615W(耐電阻)  
R=1/16W=0.062W



## EMI



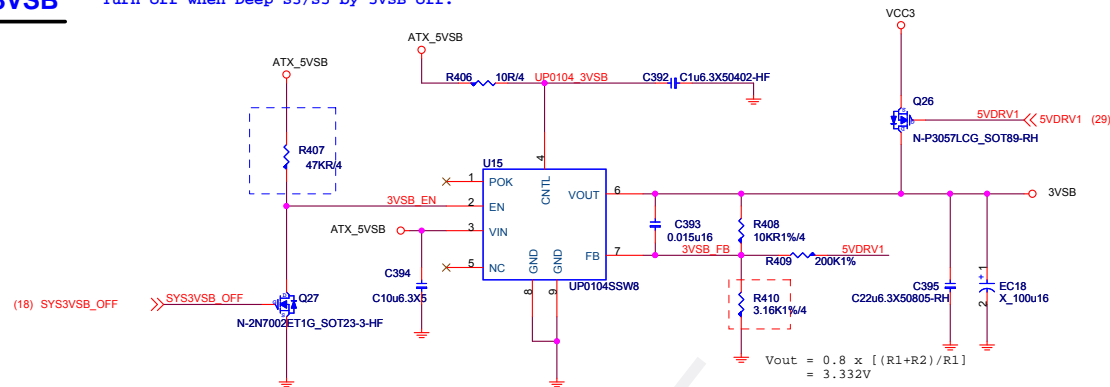
MICRO-STAR INT'L CO.,LTD

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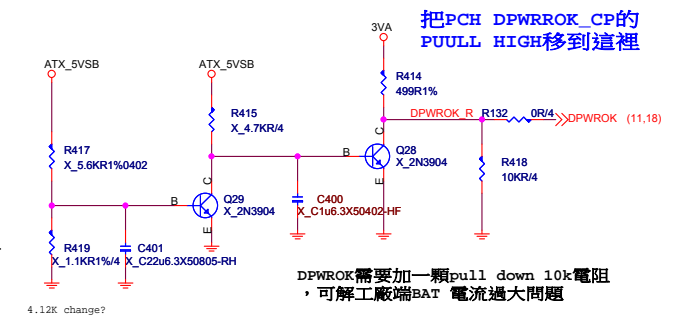
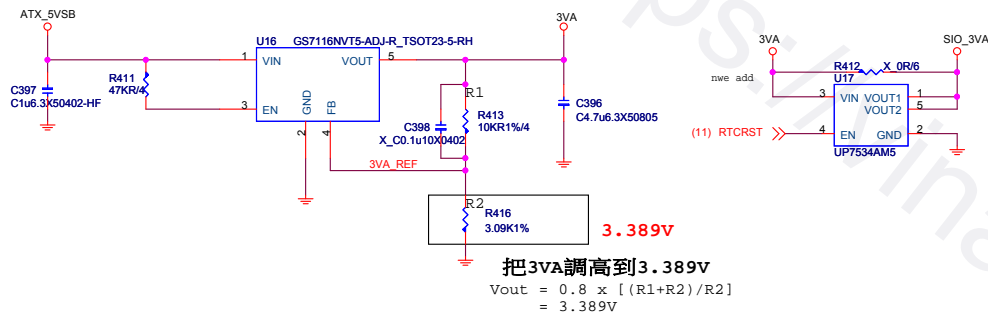
### 3VSB

3VSB supply to PCH and other device.  
Turn off when Deep S3/S5 by 5VSB off.



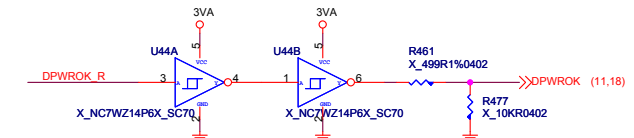
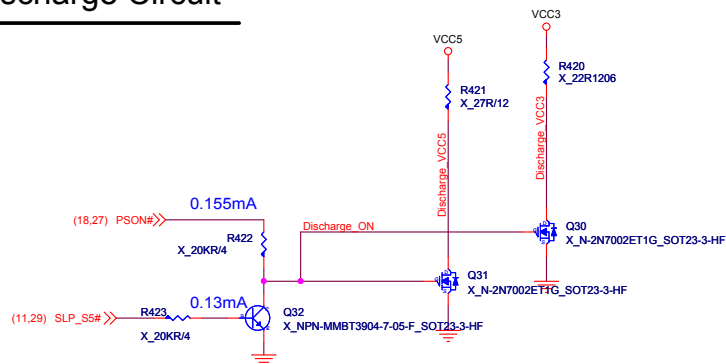
3VA

20mA



FOR DPWROK跟3VA的POWER  
DOWN的時序(S5-->G3)

## Discharge Circuit



With Deep Sx Support, Power well isolation roles of the traditional RSMRST# is replaced with DPWROK. DPWROK must be asserted for at least 10 ms after all deep sleep well is valid. DPWROK must transition from 20% signal level to 80% signal level and vice versa in 50  $\mu$ s or less.



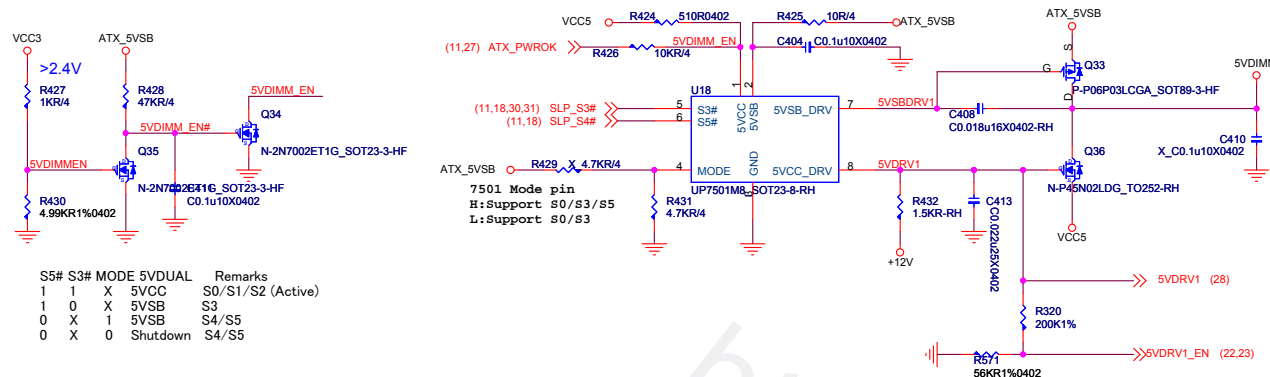
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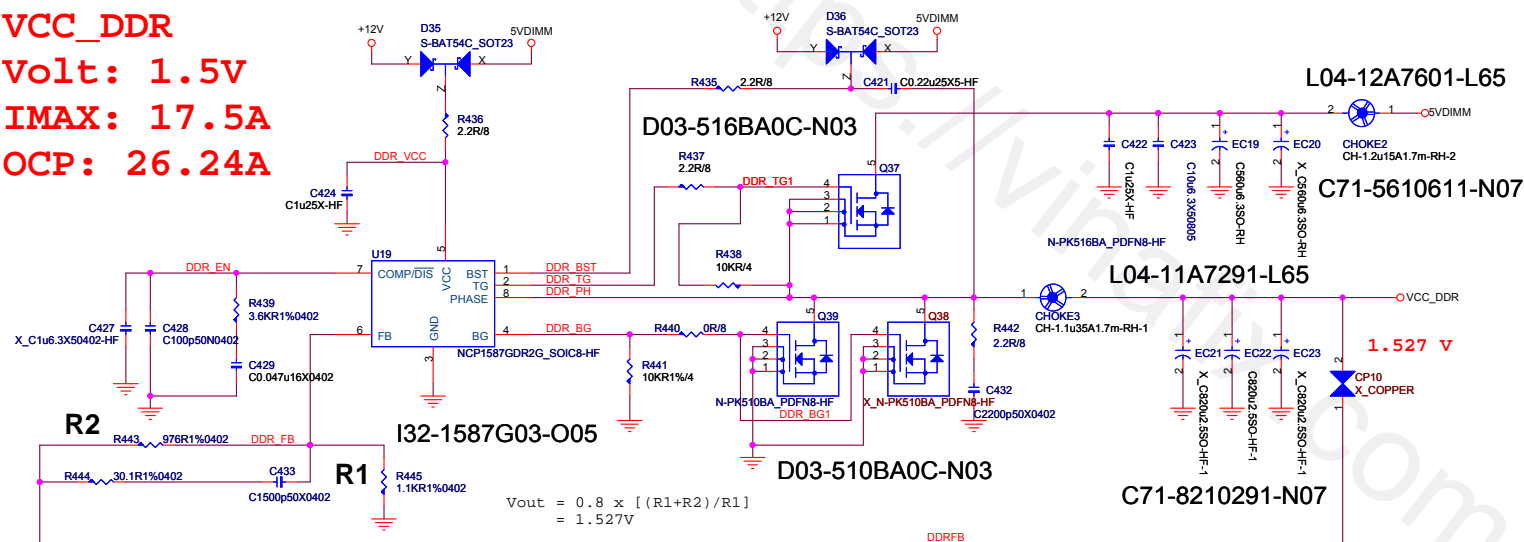
### DDRIII Regulator Power Source

**5V - 5.8A - 29W**

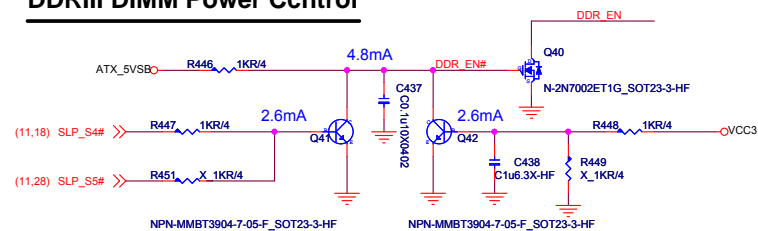

$$12 * (56 / 256) = 2.625V$$

## DDRIII DIMM Power

VCC\_DDR  
Volt: 1.5V  
IMAX: 17.5A  
OCP: 26.24A

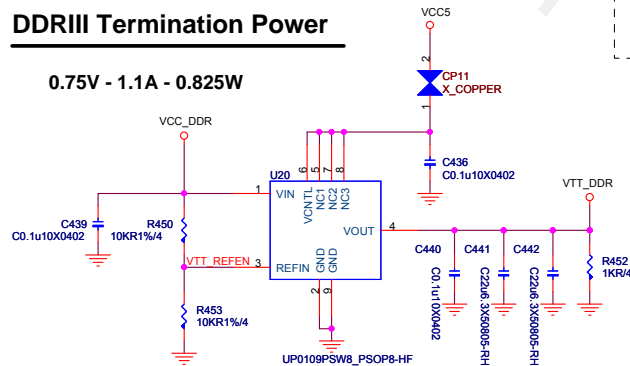


## DDRIII DIMM Power Ccntrol

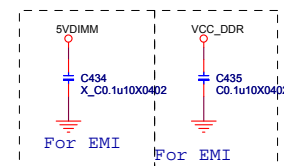
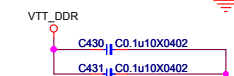
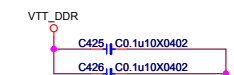
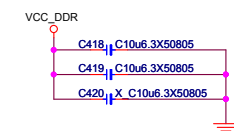
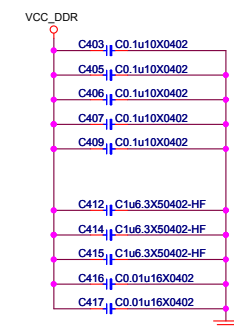
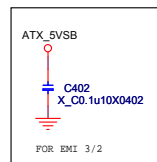


### DDRIII Termination Power

**0.75V - 1.1A - 0.825W**



**DDRIII I/O power decoupling caps.**



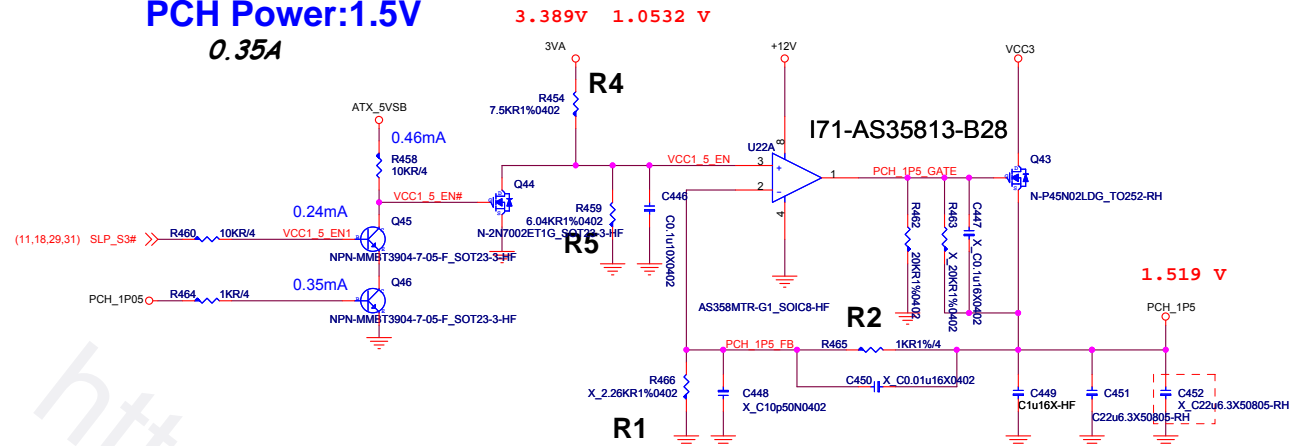
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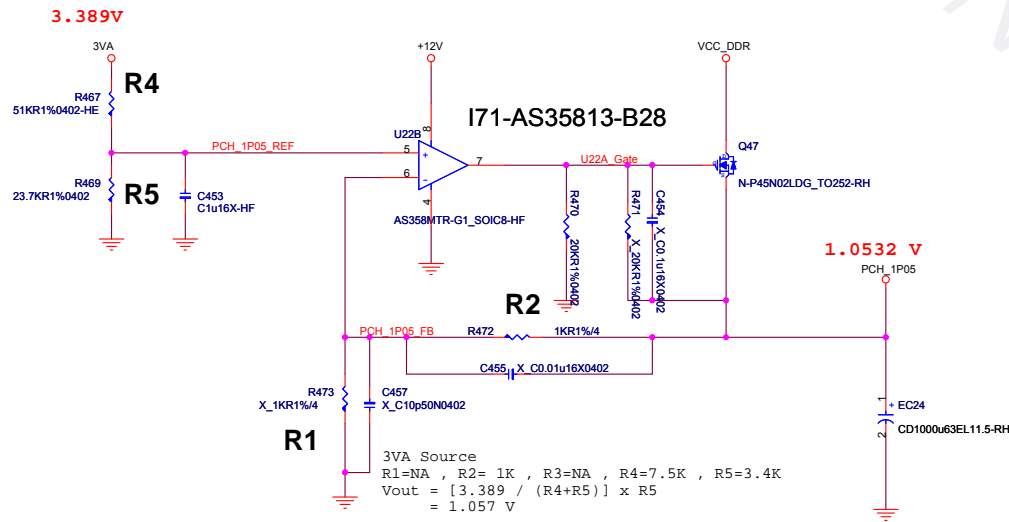
**PCH Power:1.5V**  
**0.35A**



3VA Source  
R1=NA , R2= 1K , R3=NA , R4=7.5K , R5=6.04K  
Vout = [3.389 / (R4+R5)] x R5  
= 1.512 V

**PCH\_1P5**  
**Volt: 1.5V**  
**IMAX: 0.253A**  
**PMAx: 0.3W**

**PCH Power:1.05V**  
**PCH Core 7.621A**



**PCH\_1P05**  
**Volt: 1.05V**  
**IMAX: 6A**  
**PMAx: 2.7W**

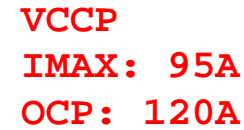
3VA Source  
R1=NA , R2= 1K , R3=NA , R4=7.5K , R5=3.4K  
Vout = [3.389 / (R4+R5)] x R5  
= 1.057 V



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**VRM Power Sequence**

ATX\_SVSB

VR\_EN

VR\_EN GD

Q48

N-2N7002ET1G\_SOT23-3-HF

R536 10KΩ/4

0.48mA

Q49

0.26mA

R537 10KΩ/4

SLP\_S3# (11,18,29,30)

R538 604R1%0402

Q50

N-2N7002ET1G\_SOT23-3-HF

R539 100R1%4

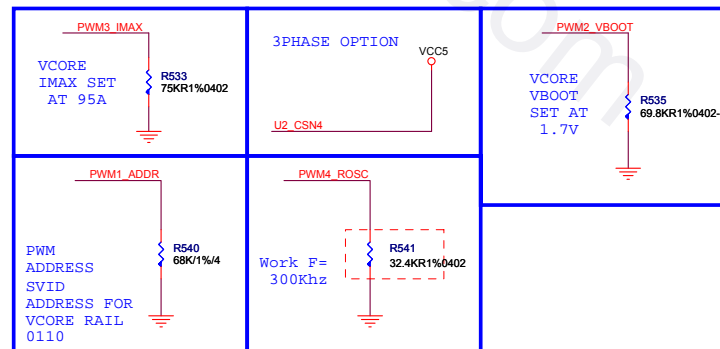
C483 C0.1u10X0402

VCC3

SYS\_PWROK (11)

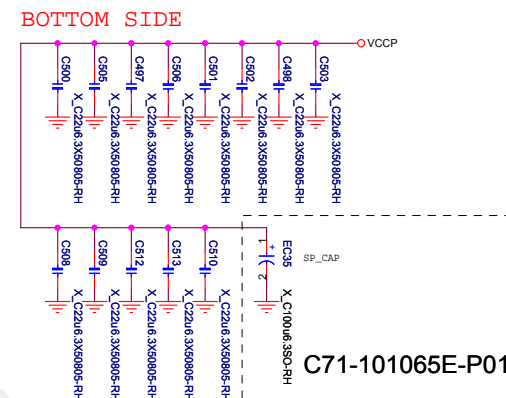
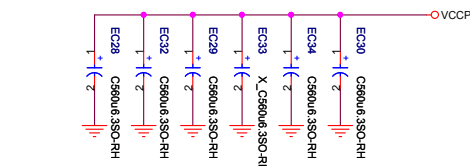
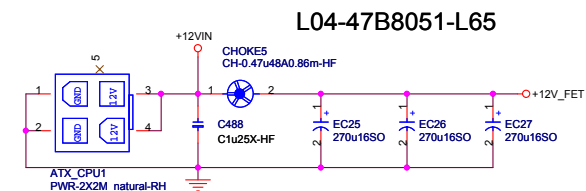
SYS\_PWROK

## CFG



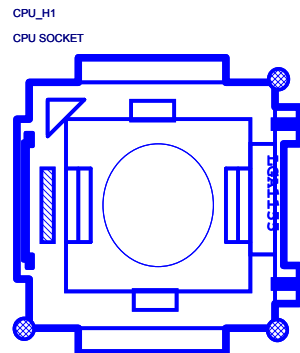
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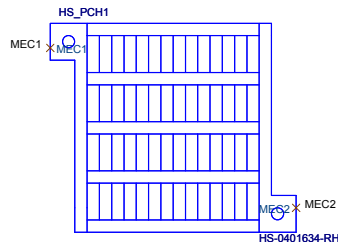


P80-0787811-G37  
P80-0787811-E48

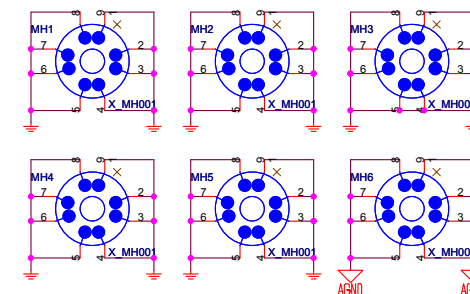


E21-7557050-L06

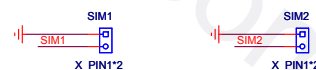
### PCH XDP PWRGD/RESET



### Mounting Holes



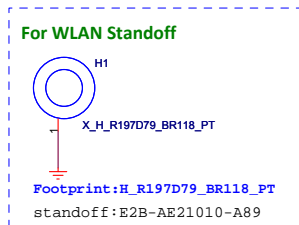
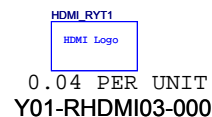
### Simulation



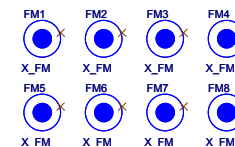
### LABEL



### HDMI VIRTUAL PN



### Optical Fiducial Marks-120



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